Meeting Ethernet Return Loss Requirements with the KTA1550

Overview

The KTA1550 provides low-capacitance Ethernet line loading to minimize the impact on twisted pair return loss performance.

Return Loss is a useful measure of the reflected power at the junction of a transmission line and terminating impedance. A low (negative dB) value of return loss represents lower reflected (lost) power and higher forward transmission in a communication system.

Return Loss, as specified in the IEEE 802.3 Ethernet standard, is a system level specification at the RJ45 interface. The Ethernet interface is specified to match the 100Ω characteristics impedance of the UTP cable. The standard requires designs to meet the return loss specification with reference impedance in the range of 85Ω - 115Ω to ensure operation over wide range of installed UTP cables. Measurement is specified to be between 1MHz-80MHz for Fast Ethernet (FE) interfaces and 1MHz-100MHz for Gigabit Ethernet (GbE) interfaces.

This document discusses Return Loss Basics and Modeling, as well as Transformer Leakage Inductance Effects. Readers interested in implementation details are encouraged to review the Design Recommendations section of this document beginning on Page 6.

Return Loss Basics

Table 1 and Figure 1 below show the required return loss specifications as per the 802.3 standards. As seen from the table and plot, critical template points for FE (100M) are 30MHz and 80MHz, and for GbE (1000M) are 40MHz and 100MHz.

Table 1. 802.3 Return Loss Specs

Freq (MHz)	802.3 Specs (dB)		
	10M	FE	GbE
1		-16.0	-16.0
5	-15.0	-16.0	-16.0
10	-15.0	-16.0	-16.0
20		-16.0	-16.0
30		-16.0	-16.0
40		-13.5	-16.0
50		-11.6	-14.1
60		-10.0	-12.5
70		-10.0	-11.2
80		-10.0	-10.0
90			-9.0
100			-8.1

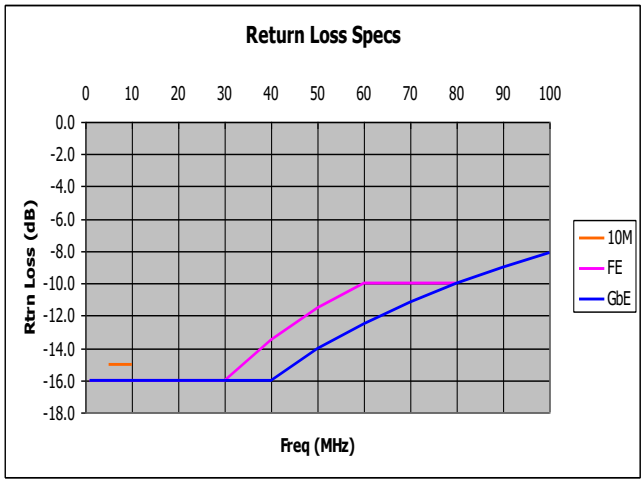


Figure 1. 802.3 Based Return Loss Templates

A simple analysis can be done to understand bounds on the problem.

$$RL = 20\log_{10}\left|\frac{Z_{ref} - Z_{DUT}}{Z_{ref} + Z_{DUT}}\right|$$

$$Z_{DUT} = Z_{ref} \times \left[\frac{1-10\text{^}(RL/20)}{1+10\text{^}(RL/20)}\right] \quad OR \quad Z_{DUT} = Z_{ref} \times \left[\frac{1+10\text{^}(RL/20)}{1-10\text{^}(RL/20)}\right]$$

From the above basic equations, and for different values of Zref as required by the standard, we can calculate the max allowable capacitance (first Z_{DUT} equation above) or inductance (second Z_{DUT} equation above) to meet the return loss requirements.

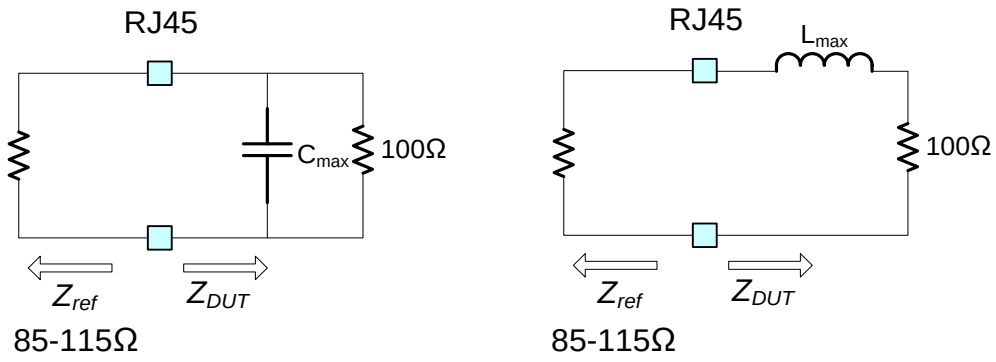


Figure 2. Simplified Circuit to Determine Max Parasitic C/L

Assuming circuit impedance is purely capacitive, Table 2 shows calculations for both FE and GbE for 2 resulting critical frequencies – the corner freq of 30/40MHz and end freq of 80/100MHz.

Table 2. Cmax Calculation for Simple Model

	Freq (Mhz)	RL	Parameter	Z_{ref} (Ω)		
				85	100	115
GbE	100	-8	Z_{DUT} (Ω)	36.6	43.1	49.5
			Z_{cap} (Ω)	57.7	75.6	98.1
			Cmax (pF)	27.6	21.1	**16.2**
	40	-16	Z_{DUT} (Ω)	61.7	72.6	83.5
			Z_{cap} (Ω)	161.4	265.5	507.3
			Cmax (pF)	24.7	15.0	**7.8**
FE	80	-10	Z_{DUT} (Ω)	44.2	51.9	59.7
			Z_{cap} (Ω)	79.1	108.1	148.4
			Cmax (pF)	25.2	18.4	**13.4**
	30	-16	Z_{DUT} (Ω)	61.7	72.6	83.5
			Z_{cap} (Ω)	161.4	265.5	507.3
			Cmax (pF)	32.9	20.0	**10.5**

As seen from Table 2, the constraint comes when the cable impedance is 115Ω. In this case the max allowable capacitance is 10.5pF for FE and 7.8pF for GbE. The 30/40MHz corner frequency is the closest violation point that determines maximum allowable capacitance.

Similarly, we can analyze the channel for max allowable inductance in the Device Under test (DUT) to meet the return loss requirements. In this case the constraint comes when the cable impedance is 85Ω. As seen in Table 3, the max allowable inductance is 156nH for FE at 80MHz, and 127nH for GbE at 40MHz.

Table 3. Lmax Calculation for Simple Model

	Freq (Mhz)	RL	Parameter	Z_{ref} (Ω)		
				85	100	115
GbE	100	-8	Z_{DUT} (Ω)	197.4	232.3	267.1
			Z_{cap} (Ω)	112.4	132.3	152.1
			Lmax (nH)	**179**	211	242
	40	-16	Z_{DUT} (Ω)	117.0	137.7	158.3
			ZL (Ω)	32.0	37.7	43.3
			Lmax (pF)	**127**	150	172
FE	80	-10	Z_{DUT} (Ω)	163.6	192.5	221.4
			ZL (Ω)	78.6	92.5	106.4
			Lmax (pF)	**156**	184	212
	30	-16	Z_{DUT} (Ω)	117.0	137.7	158.3
			ZL (Ω)	32.0	37.7	43.3
			Lmax (pF)	**170**	200	230

These capacitance and inductance numbers are very much in the range of parasitic loading that is provided by transformers, transceivers and other components that are part of the media interface.

DUT Model

The simplest way to analyze return loss in a real DUT is to establish a distributed model of the impedance network, looking into the RJ45 interface. An Ethernet Transformer provides both inductive and capacitive parasitics. Most of the other devices like the Ethernet transceiver and ESD protection devices (diodes/sidactors) can be modeled as parasitic loads. PCB traces used for routing differential signals should be modeled as a 100Ω differential transmission line. However for a small section of signal traces at frequencies below 100MHz, these lines still need to be treated as lumped capacitive load elements.

Figure 3 shows a typical KTA1550 application diagram. Here the KTA1550 is representative of any EMI/ESD protection device used in the circuit.

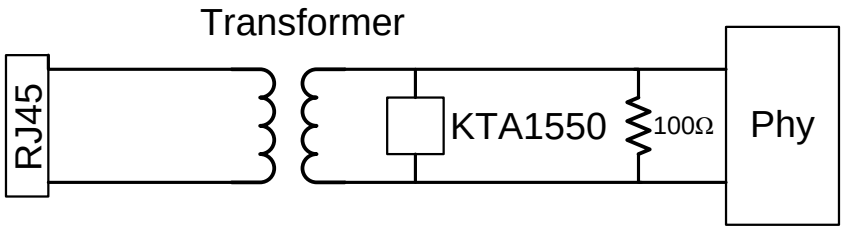


Figure 3. Simplified System Model

Transformer Model

Figure 4 shows the model of a typical Ethernet transformer. This model is based on measured data of popular 10/100M transformers, and as a lumped element model captures the parasitic circuit elements of the differential transformer as well as the common-mode choke (looking into the Ethernet transceiver).

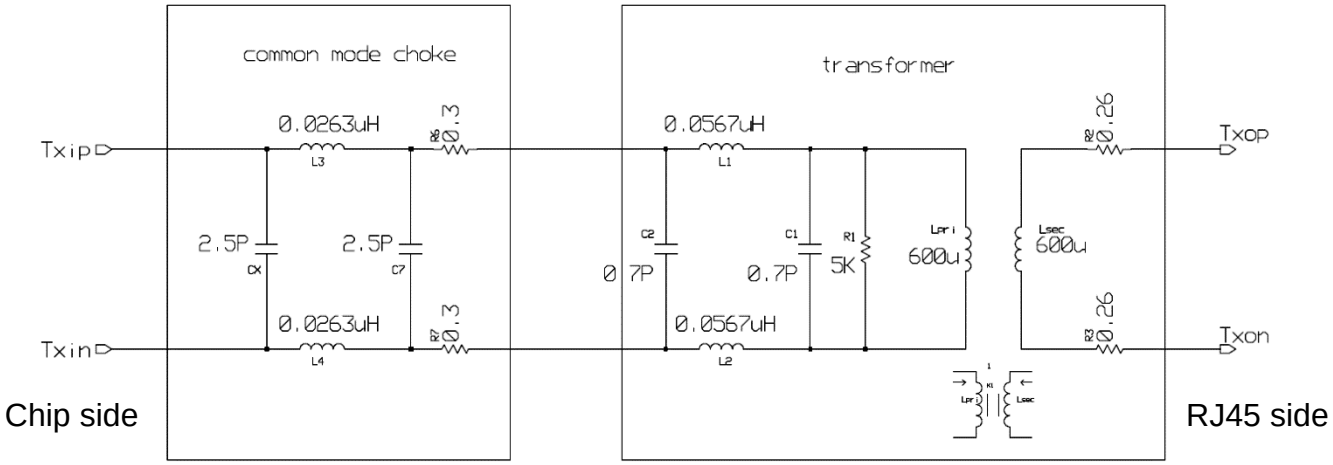


Figure 4. Typical Transformer Model for Differential-mode Analysis

Leakage inductances and parasitic capacitances are the critical parameters for return loss analysis. Total leakage inductance of this typical Ethernet transformer is 165nH and the total differential parasitic capacitance is 6.4pF. These numbers are within the range of Cmax and Lmax, as previously computed in Tables 2 and 3.

Analyzing the Effect of Transformer Leakage Inductance

As noted, the return loss analysis is a multi-variable problem and often datasheet information on many variables is not available. But another way to analyze the problem is to determine the range of acceptable transformer leakage inductance and the Ferrite bead inductance that will produce an appropriate solution.

Fixed parameters:

Cphy = 5pF, C1602 = 4.5pF,

Cpcb3 = 1.5pF, Cpcb1 = 0pF, Cpcb2 = 5pF (diff)

C-xfrmr-total = 19pF (note: this is made very high for illustration purpose)

The following graphs show the resulting ranges of acceptable Xfrmr leakage inductance vs. ferrite bead inductance to meet FE return loss requirements. Figure 5 shows ranges when the common mode choke is placed on the chip side. Conversely, Figure 6 shows the ranges when the common mode choke is placed on the line side. Similar analysis can be done for GbE.

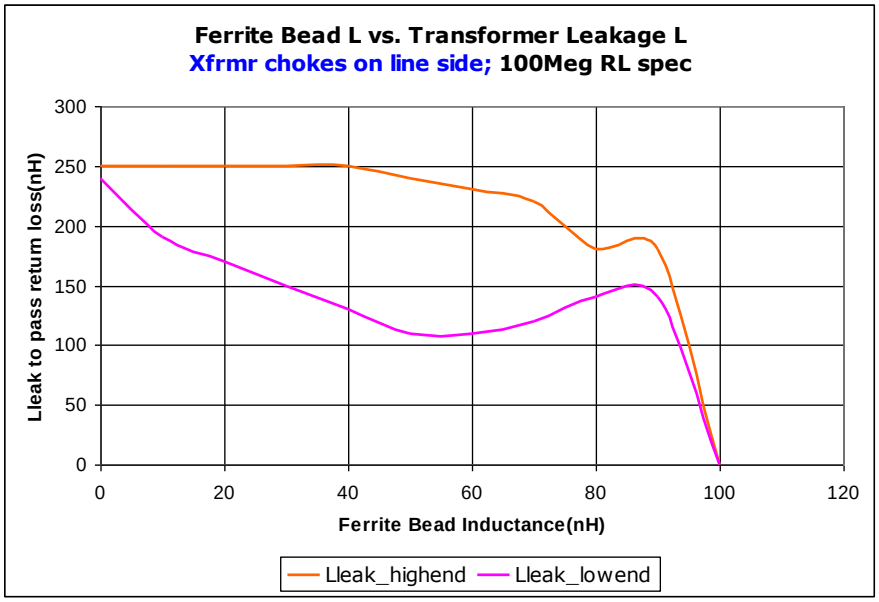


Figure 5. Xfrmr Choke on the Chip Side: FB vs Xfrmr Leakage

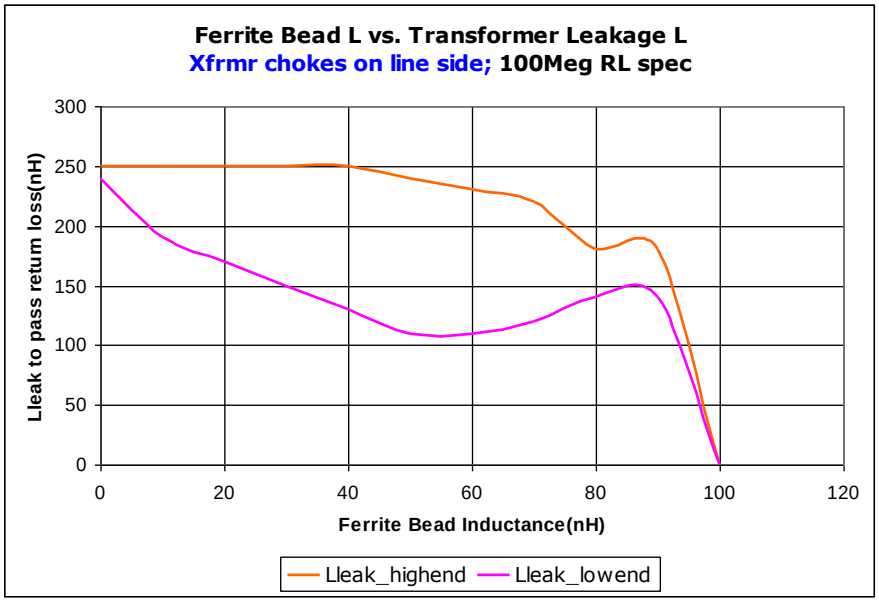


Figure 6. Xfrmr Choke on the Line Side: FB vs. Xfrmr Leakage

Purely from a return loss perspective, having a transformer with chokes on the line side is preferred since it inserts the transformer leakage inductance between the choke inter-winding capacitance and the rest of the system, creating a better distributed network for return loss. However other considerations should be kept in mind while choosing the choke locations. Specifically, current saturation in Power Over Ethernet (POE) systems and the potential for higher cross-talk in GbE systems when multiple chokes are wound on same cores to cancel DC currents in the POE network.

Design Recommendations

The KTA1550 is designed for low capacitance loading on the line, providing a low impact to the resulting Ethernet return loss performance. Additionally, the KTA1550 can be used with off-the-shelf Ethernet transceivers and transformers to meet the required return loss specifications.

However, given the number of system parameters that can impact return loss, it's not always possible to predict the performance and variation due to used components. Therefore it is recommended that ferrite beads also be used as means of tuning the return loss performance at the system level.

Ferrite Bead Implementation

To realize the needed inductance (10-90nH range), use of ferrite beads is recommended. Ferrite beads are much cheaper than equivalent inductors. In the frequency range of interest, the real part of the impedance is negligible as shown in Figure 7. In the out-of-band spectrum (beyond 100MHz), the real part of the bead's impedance actually creates a low-pass filtering effect that helps filter out high-frequency harmonics and improves EMI performance.

An appropriate choice of ferrite bead is the Murata BLM18B series (0603), which is meant for high speed signal lines with low DCR values. Ferrite bead impedance is typically rated at 100MHz. The range of usable ferrite bead impedance for this application is typically 10Ω to 47Ω, with good centering at the 22Ω value (BLM18BA220SN1 or BLM18BB220SN1). These beads are also available in the smaller 0402 size (BLM15B series).

Table 4 shows available models in the BLM18B series. Equivalent models from other vendors are also available.

http://search.murata.co.jp/Ceramy/image/img/PDF/ENG/L0110S0100BLM18B.pdf

Table 4. Catalog of Ferrite Beads from Murata

Model #	Z_{typ} @ 100MHz	Rate I	DCR	Temp Range	# of Circuits
BLM18BA100SN1	10Ω ±25%	500mA	0.25Ω	-55°C to +125°C	1
BLM18BB100SN1	10Ω ±25%	500mA	0.15Ω	-55°C to +125°C	1
BLM18BA220SN1	22Ω ±25%	500mA	0.35Ω	-55°C to +125°C	1
BLM18BB220SN1	22Ω ±25%	500mA	0.25Ω	-55°C to +125°C	1
BLM18BA470SN1	47Ω ±25%	300mA	0.55Ω	-55°C to +125°C	1
BLM18BB470SN1	47Ω ±25%	500mA	0.30Ω	-55°C to +125°C	1

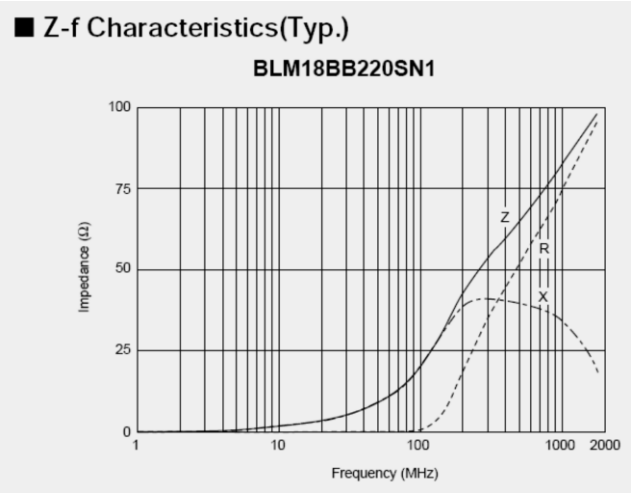


Figure 7. Impedance Characteristics of a 22Ω Ferrite Bead

There are two additional considerations associated with the use of Ferrite beads:

- The use of ferrite beads creates a low-pass filter (with 3-db cutoff frequency beyond 100MHz pass-band) that can help remove some of the high frequency harmonics from transmission on the UTP. This can improve EMI performance of the system.
- The use of ferrite beads can marginally slow down rise/fall time of the Ethernet signal. But for the values of ferrite bead considered here this will typically be in the 100pS range. Given the 3-5nS rise/fall time requirements in Ethernet Template, this will have a minimal impact.

Design Guide

Based on the above analysis, here is a consolidated design recommendation for designing an Ethernet media interface to meet return loss requirements.

1. Place all MDI signal path components on the same board side to avoid pcb vias. Vias cause impedance discontinuity and can impact return loss. If vias can not be avoided, match the number and position of vias on each member within the MDI signal pair. This is more of an issue for GbE that has a more stringent return loss requirement. Note that the KTA1550 package is designed to allow through routing that eliminates via drops.
2. Use a controlled impedance, microstrip traces with solid ground under signal traces. Each of the MDI differential ("+" and "-") traces should have a 50-ohm characteristic impedance to ground, 100 ohms between each other, and trace lengths matched within 50 mils.
3. Place the components as close together as mechanically possible to minimize differential signal lengths. Always place the Ethernet termination resistors (50Ω) very close to the transceiver.
4. Use a transformer as recommended by the transceiver vendor. Transformers with chokes on the line side (towards the RJ45) will have better return loss performance. However please review the transceiver-transformer compatibility guide provided by the transceiver vendor to make sure such transformer is usable.
5. Place recommended ferrite beads on the differential signals between KTA1550 and the Ethernet transceiver. Locate the ferrite beads near the transceiver, after the Ethernet termination resistors.
6. In the lab test for return loss, pulse template, and high frequency EMI noise to fine-tune the value of ferrite bead. For better EMI performance, use the largest ferrite bead (within a 10-47Ω range) that allows the system to pass return loss and does not impact the pulse template. Note that if the layout is really compact, ferrite beads may not be needed and can be replaced with a 0Ω stuff option or designed out in a later board rev.
7. For GbE: spacing between the channels controls the inductive crosstalk and should be at least twice the spacing between the members of each pair in a channel.

Summary

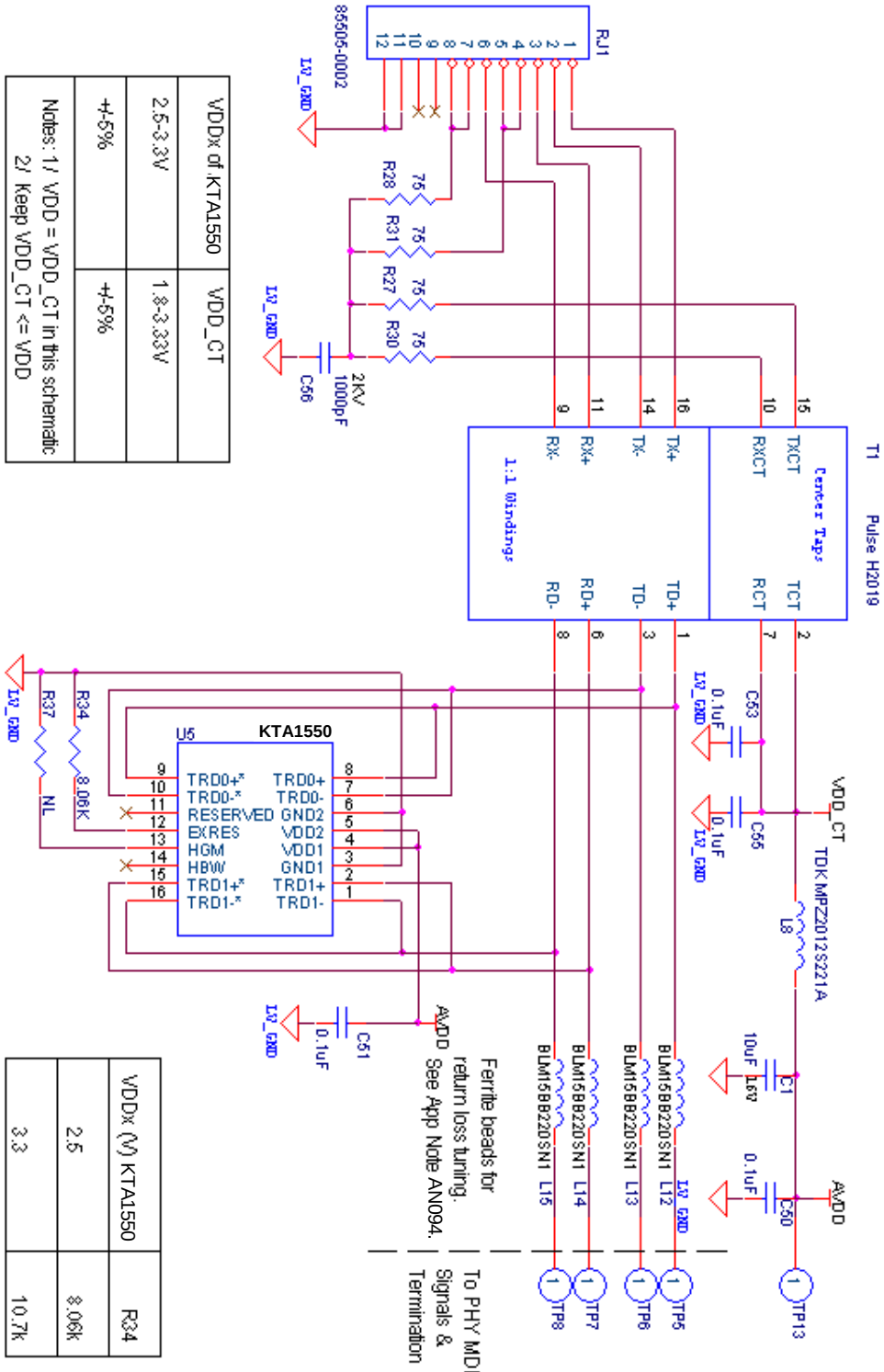
Meeting return loss templates is not always trivial due to the complex nature of the impedance network between the RJ45 connector and the Ethernet termination impedance on the board.

The KTA1550 provides low-capacitance loading on the line and therefore will have a have low impact on Ethernet return loss. Given the many unknown variables and parameters it is recommended to use ferrite beads as part of the design. The beads provide the ability to fine-tune the return loss and high-frequency EMI performance of the system.

These guidelines will give system designers a quick path to meet Ethernet return loss requirements without requiring a custom transformer design or board re-layout.

Appendix: Recommended Application Schematics

FE Reference Schematic

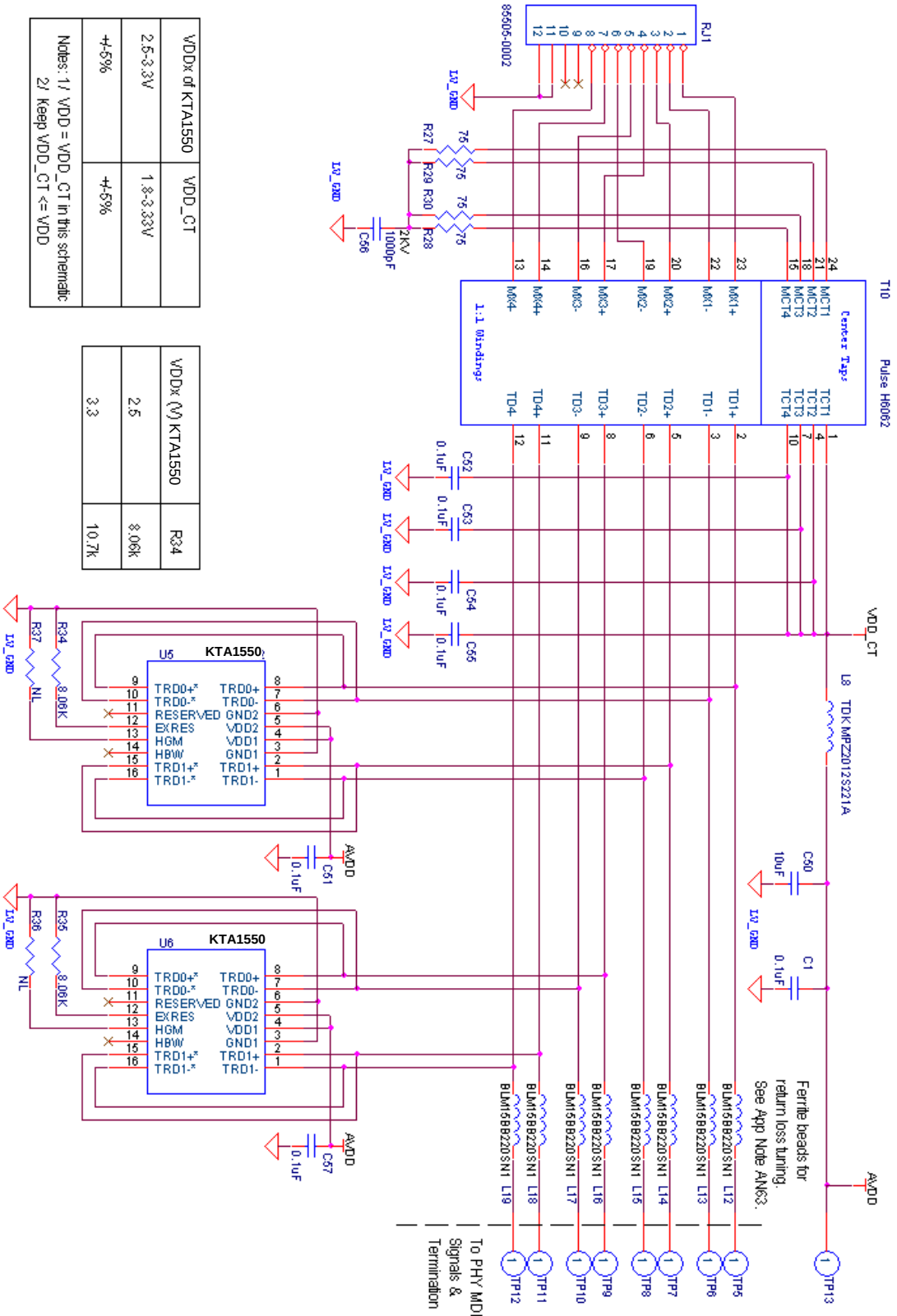


VDDx of KTA1550	VDD_CT
2.5-3.3V	1.8-3.33V
+/-5%	+/-5%

Notes: 1/ VDD = VDD_CT in this schematic
2/ Keep VDD_CT <= VDD

VDDx (V) KTA1550	R34
2.5	8.06k
3.3	10.7k

GbE Reference Schematic



Related Documentation

1. Kinetic Technologies Datasheet: KTA1550 Datasheet
2. Kinetic Technologies Application Note: AN93 – KTA1550 Design Guide
3. Murata Datasheet: Noise Suppression Products – EMI Suppression Filters, L0110S0100BLM03A, March 2005
4. IEEE Standard: IEEE Std 802.3at™-2009, October 2009