EPR 48V 6A$_{RMS}$ VBUS OVP Load Switch with Surge Protection

Features

- 3V to 55V Operating Voltage Range
- 56V$_{DC}$ Abs. Max. Rating at VBUS and 59V$_{DC}$ at VSYS
- 6A$_{RMS}$ Continuous Current Rating
- 31mΩ typ. On-Resistance from VBUS to VSYS
- 54V, 300ns Over-Voltage Protection (OVP) at VBUS
  - ▶ 4V to 55V External Resistor Programmable
- Over-Voltage Protection (OVP) latch off at VCHSYS
  - ▶ 4V to 55V External Resistor Programmable
- Transient Voltage Suppression (Active TVS) at VBUS
  - ▶ ±130V Surge Protection (IEC61000-4-5, I_{PP}=34A)
  - ▶ ±30kV ESD Contact Discharge (IEC61000-4-2)
  - ▶ ±30kV ESD Air-Gap Discharge (IEC61000-4-2)
- Soft-Start (SS) Limits Inrush Current
- Short-Circuit Protection (SCP) during & after SS
- 24A, 200ns Over-Current Protection (OCP)
- "Ideal Diode" Reverse-Current Protection (RCP, KTS1801A only)
  - ▶ V_F = 17mV and 15µs Fast Recovery
- Bi-directional Mode when enabled (KTS1801B only)
- Over-Temperature Protection (OTP)
- VBUS Active Discharge Circuit
- $\overline{\text{ACOK}}$ Output Flag & Hiccup Auto-Retry after Faults
- -40°C to 85°C Operating Temperature Range
- 42-bump WLCSP 3.09 x 3.86mm (0.5mm pitch)

Brief Description

The KTS1801 is a USB VBUS safety management load switch for up to 288W input or output in 48V EPR systems. The operating range is 3V to 55V with VBUS withstand up to 56V$_{DC}$ and VSYS up to 59V$_{DC}$. Ultra-fast over-voltage protection (OVP) is internally set to 54.2V, but optionally adjusted via external resistors. Low on-resistance minimizes heat and voltage droop.

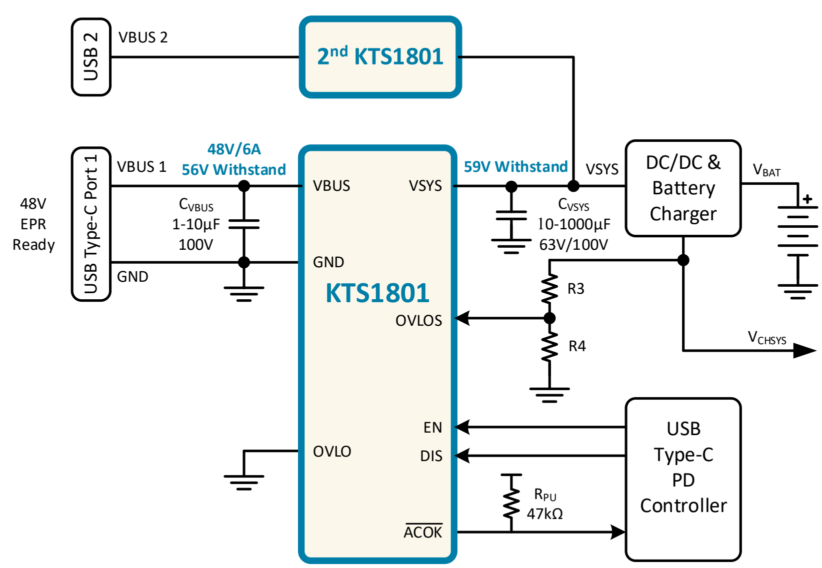
KTS1801A has automatic reverse-current protection (RCP) feature which acts as a 17mV "ideal diode" with fast recovery. KTS1801B supports bi-directional mode when enabled. Additional safety management includes short-circuit protection (SCP) during and after soft-start, ultra-fast over-current protection (OCP), over-temperature protection (OTP), and an integrated transient voltage suppressor (Active TVS) for IEC industry standard ±30kV ESD and ±130V surge ratings. VBUS active-discharge circuits is also integrated.

The KTS1801 is packaged in advanced, fully "green" compliant, 3.09 x 3.86mm, 42-bump Wafer-Level Chip-Scale Package (WLCSP).

Applications

- Workstation & Gaming Notebooks
- Mini Desktop PCs, Monitors, Docking Stations
- Conferencing Systems
- Tools, E-Bikes, Battery Power Stations, etc.

Typical Application

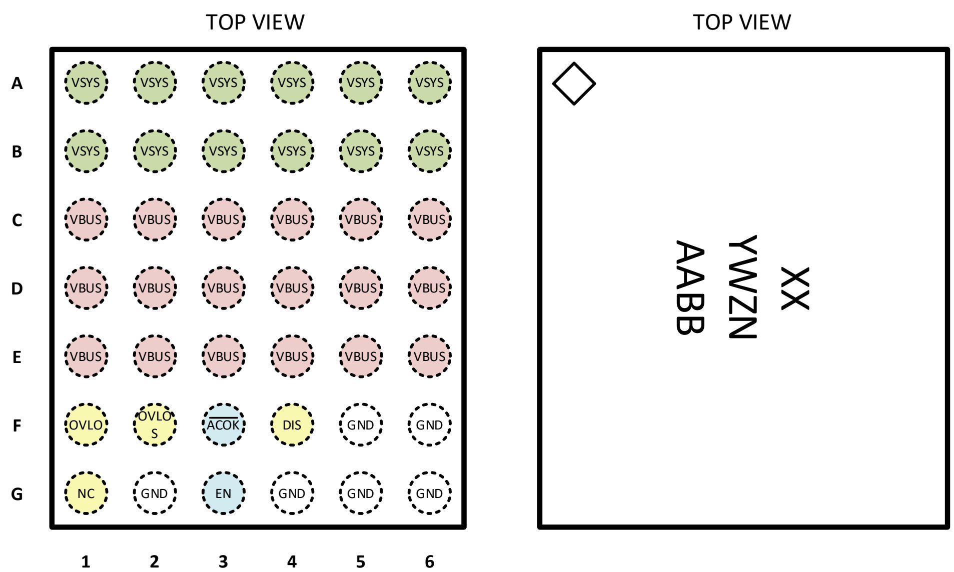


Ordering Information

Part Number	Marking[1]	Switch Mode	Package
KTS1801AEMAB-TB	VOYWZNAABB	Uni-directional with RCP	WLCSP-42
KTS1801BEMAB-TB[2]	VPYWZNAABB	Bi-directional without RCP	WLCSP-42

Pinout Diagram

WLCSP76-42



42-bump 3.09 x 3.86mm x 0.555mm
WLCSP Package, 0.500mm pitch

Top Mark
XX = Device Code
YW = Date Code, ZN = Assembly Code
AABB = Serial Number

1. VO, VP = Device Code, YW = Date Code, ZN = Assembly Code, AABB = Serial Number.

2. Consult Kinetic Technologies authorized representative for availability.

Pin Descriptions

Pin #	Name	Function
A1 to B6	VSYS	Power Switch System-Side Connection – connect to switching regulator output, battery charger input, and/or switching regulator input for systems without rechargeable batteries.
C1 to E6	VBUS	Power Switch VBUS Port-Side Connection – connect to VBUS on USB port.
F1	OVLO	External OVLO Adjustment – connect to GND to use the internally fixed OVP threshold. Connect an external resistive voltage divider from VBUS to OVLO to GND to set an adjustable OVLO threshold.
F2	OVLOS	OVLOS Adjustment – Connect an external resistive voltage divider from VCHSYS to OVLOS to GND to adjust the OVLOS threshold. Connect to GND if not used.
F3	$\overline{\text{ACOK}}$	Power Good Flag – active-low, open-drain logic output. Connect to GND or leave floating if unused.
F4	DIS	V_{BUS} Active Discharge Input – active-high analog input with internal 1MΩ pull down; connected to gate of internal V_{BUS} active discharge FET.
G1	NC	No connect pin. Must leave it be floated if needs to co-layout with KTS1800. Or connect it to GND if there is no any special purpose.
G3	EN	Enable – active-high logic input
F5, F6 G2, G4 to G6	GND	Ground

Absolute Maximum Ratings[3]

Symbol	Description	Value	Units
V_{BUS}	VBUS to GND (continuous)	-0.3 to 56	V
	VBUS to GND (during IEC61000-4-5 surge event)[4]	-5 to 64	
V_{SYS}	VSYS to GND	-0.3 to 59	V
$V_{BUS-SYS}$	VBUS to VSYS	-59 to 56	V
V_{OVLO}, V_{OVLOS}	OVLO, OVLOS to GND (Current from VBUS or VCHSYS through R1 or R3 to these pins is less than 2mA, R1 or R3 > 10KΩ)	-0.3 to 12	V
V_{EN}, V_{DIS}, $V_{\overline{ACOK}}$	EN, DIS, $\overline{ACOK}$ to GND	-0.3 to 6	V
I_{SW}	Maximum Switch Current (continuous)	6	A
	Peak Switch Current (5ms, OCP and Pd limited)	20	
T_J	Die Junction Operating Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-55 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD and Surge Ratings[5]

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC JS-001-2017 Human Body Model (all pins)	±2	kV
V_{ESD_CD}	IEC61000-4-2 Contact Discharge (VBUS)	±30	kV
V_{ESD_AGD}	IEC61000-4-2 Air Gap Discharge (VBUS)	±30	kV
V_{SURGE}	IEC61000-4-5 Surge (V_{BUS} = 0V_{DC}+Surge, C_{VBUS} = 0µF)	±130	V
	IEC61000-4-5 Surge (V_{BUS} = 48V_{DC}+Surge, C_{VBUS} = 10µF, R_{LOAD} = 400Ω)	±80	V
	IEC61000-4-5 Surge (V_{SYS} = 0V_{DC}+Surge, C_{VSYS} = 0µF)	±66	V

Thermal Capabilities[6]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	36	°C/W
P_D	Maximum Power Dissipation at $T_A \leq 25°C$ ($T_J \leq 125°C$)	2.78	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-27.8	mW/°C

3. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.

4. The internal active TVS FET and main NMOSFET on the VBUS pin can withstand up to +64V peak pulse voltage (duration is less than 100µs) based on process standard. The internal active TVS can clamp VBUS voltage up to less than 63V during IEC61000-4-5 +130V surge event.

5. ESD and Surge Ratings conform to JEDEC and IEC industry standards. Some pins may actually have higher performance. Surge ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.

6. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.

Recommended Operating Conditions[7]

Symbol	Description	Value	Units
V_{BUS}, V_{SYS}	VBUS, VSYS Operating Voltage	3 to 55	V
V_{EN}, V_{DIS}, V_{OVLO}, V_{OVLOS}	EN, DIS, OVLO, OVLOS Input Voltage	0 to 5.5	V
$V_{\overline{ACOK}}$	$\overline{ACOK}$ Flag Output Pull-Up Voltage	0 to 5.5	V
T_A	Ambient Operating Temperature Range	-40 to 85	°C
T_J	Die Junction Operating Temperature Range	-40 to 125	°C
C_{VBUS}	VBUS External Local Capacitance	1 to 10	µF
		100	V
C_{VSYS}	VSYS External Capacitance	10 to 2240	µF
		63 or 100	V
T_A	Ambient Operating Temperature Range	-40 to 85	°C
T_J	Die Junction Operating Temperature Range	-40 to 125	°C

Electrical Characteristics[8]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_J = -40°C to +125°C with V_{BUS} = 3V to 55V or V_{SYS} = 3V to 55V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V or V_{SYS} = 5V.

Supply Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{BUS}	VBUS Supply Operating Voltage Range		3		55	V
V_{SYS}	VSYS Supply Operating Voltage Range		3		55	V
V_{UVLO}	Under-Voltage Lockout	V_{BUS} rising threshold		2.7	2.95	V
		V_{SYS} rising threshold (KTS1801B)		2.7	2.95	V
		Hysteresis		400		mV
I_Q	No-Load Supply Current (Enabled)	V_{BUS} = 5V, V_{SYS} = open		350		µA
		V_{BUS} = 48V, V_{SYS} = open		620		
	No-Load Supply Current (Enabled, KTS1801B in I_{SOURCE} Mode)	V_{SYS} = 5V, V_{BUS} = open		350		
		V_{SYS} = 48V, V_{BUS} = open		620		
I_{SHDN}	Shutdown Supply Current	V_{BUS} = 5V, V_{SYS} = open		2		µA
		V_{BUS} = 48V, V_{SYS} = open		7		
	Shutdown Supply Current (KTS1801B in I_{SOURCE} Mode)	V_{SYS} = 5V, V_{BUS} = open		2		
		V_{SYS} = 48V, V_{BUS} = open		7		
I_{Q_RCP}	Output Supply Current in RCP (KTS1801A)	Enabled, V_{BUS} = 0V, V_{SYS} = 5V		140		µA

(continued next page)

7. The recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Kinetic does not recommend exceeding them or designing to Absolute Maximum Rating.

8. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.

Electrical Characteristics (continued)[9]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_J = -40°C to +125°C with V_{BUS} = 3V to 55V or V_{SYS} = 3V to 55V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V or V_{SYS} = 5V.

Active TVS Surge Clamp Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{TVS_WRK}	Maximum Working Voltage	Positive Working Voltage			55.5	V
		Negative Working Voltage[10]	-0.3			
V_{TVS_BR}	Reverse Breakdown Voltage	I_{IN} = 10mA	56.5	58.3	60.1	V
V_{TVS_F}	Forward Voltage	I_{IN} = -10mA[10]	-2	-0.6	-0.3	
V_{TVS_CLAMP}	Clamping Voltage[10] (V_{BUS} = 0 V before surge, C_{VBUS} = 0µF, 25°C)	15A IEC61000-4-5 Surge (8/20 µs) from VBUS to GND		60.5	63	V
		34A IEC61000-4-5 Surge (8/20 µs) from VBUS to GND		62	64	
		-100A IEC61000-4-5 Surge (8/20 µs) from VBUS to GND		-2	-5	
P_{PP}	Peak Pulse Power, 25°C[10]	130V IEC61000-4-5 Surge (8/20 µs)			2200	W

Logic Pin Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input Logic High (EN)		1.2			V
V_{IL}	Input Logic Low (EN)				0.4	V
I_{I_LK}	Input Logic Leakage (EN)	V_I = 5V	-1		1	µA
V_{OL}	Output Logic Low ($\overline{ACOK}$)	I_{O_SINK} = 1mA		0.01	0.2	V
I_{O_LK}	Output Logic High-Z Leakage ($\overline{ACOK}$)	V_O = 5V	-1		1	µA

V_{BUS} Active Discharge (DIS) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{AD}	Active Discharge Resistance (from V_{BUS}=5V to GND)	V_{DIS} = 3V	0.11	0.22	0.32	kΩ
		V_{DIS} = 2V		0.25		
		V_{DIS} = 1.5V		0.4		
		V_{DIS} = 1.4V		0.5		
		V_{DIS} = 1.2V, T_A = 0°C to +85°C		1.5	3.0	
V_{IH_DIS}	DIS Input High Voltage	R_{AD} < 3kΩ, T_A = 0°C to +85°C	1.2			V
V_{IL_DIS}	DIS Input Low Voltage[10]	R_{AD} is high-Z			0.5	V
R_{DIS_PD}	DIS Internal Pull-Down Resistor			1		MΩ
t_{VBUS_DIS}	V_{BUS} Active Discharge Time[11]	V_{BUS} = 5V, V_{DIS} = 3V, C_{VBUS} = 10µF		6		ms

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9. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization, and correlation with statistical process controls.

10. Guaranteed by design, characterization and statistical process control methods; not production tested.

11. t_{VBUS_DIS} is the time for VBUS to fall from 5V (vSafe5V) to below 0.8V (vSafe0V). The USB specification for tSafe0V is 0ms to 650ms, so in theory, this can discharge up to 1000µF in case of excessive source bulk capacitance.

Electrical Characteristics (continued)[12]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_J = -40°C to +125°C with V_{BUS} = 3V to 55V or V_{SYS} = 3V to 55V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V or V_{SYS} = 5V.

Power Switch Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{ON}	Switch On-Resistance in I_{SINK} mode T_A = +25°C	V_{BUS} = 5V, I_{SYS} > 1.0A		31		mΩ
		V_{BUS} = 48V, I_{SYS} > 1.0A		31	38	
	Switch On-Resistance in I_{SOURCE} mode T_A = +25°C (KTS1801B)	V_{SYS} = 5V, I_{BUS} > 1.0A		31		
		V_{SYS} = 48V, I_{BUS} > 1.0A		31	38	
I_{BUS_OFF}	Switch Off-Leakage at VBUS[10] (tested in shutdown mode)	V_{BUS} = 0V, V_{SYS} = 3V to 55V, dark	-10	-0.001	10	µA
I_{SYS_OFF}	Switch Off-Leakage at VSYS[10] (tested in shutdown mode)	V_{SYS} = 0V, V_{BUS} = 3V to 55V, dark	-10	-0.001	10	µA

Soft-Start (SS) Specifications (see Figure 1)

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{DEB}	Soft-Start Debounce Time[13]	V_{BUS} = 5V V_{SYS} = 5V (KTS1801B in I_{SOURCE} Mode)	10	16	25	ms
V_{SR_SS}	Soft-Start Voltage Ramp Slew-Rate	I_{SINK} or I_{SOURCE}		1		V/ms
t_R	Soft-Start Voltage Ramp Time	I_{SINK} or I_{SOURCE}, V_{BUS} or V_{SYS} = 10% to 90%		0.8*V_{BUS}		ms
I_{LIM_SS}	Soft-Start Current Limit (for SCP)	V_{BUS} = 5V		2		A
		V_{SYS} = 5V (KTS1801B in I_{SOURCE} Mode)		2		
		V_{BUS} = 48V, V_{SYS} = 0V		1		
		V_{SYS} = 48V, V_{BUS} = 0V (KTS1801B in I_{SOURCE} Mode)		1		
t_{LIM_SS}	Soft-Start Current Limit Done Time[14]	I_{SINK} or I_{SOURCE}		2		ms
t_{DOFF}	Turn-Off Delay Time[10, 15]		0	2	10	µs

$\overline{ACOK}$ Flag Recovery and Hiccup Timer Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
t_{HICCUP}	Fault Condition Hiccup Retry Time[16]	after any fault		64		ms
$t_{\overline{ACOK}}$	Power Good Delay after t_{LIM_SS}	after t_{LIM_SS}		2		ms

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12. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.
13. t_{DEB} is time from enabled logic and valid supply voltage until the output voltage begins to rise.
14. t_{ILIM_SS} is time from when the output voltage exceeds the input voltage minus 0.9V until the soft-start current limit ends.
15. t_{DOFF} is time from enable logic until the output voltage begins to fall.
16. Faults include OVP, OTP, OCP, and SCP. After the fault condition has ended, the hiccup timer triggers, followed by the soft-start sequence, and then the $\overline{ACOK}$ flag is pulled low to indicate the power is good. The RCP is not classified as fault, it doesn't trigger the $\overline{ACOK}$ flag and hiccup timer. RCP has fast recovery without initiating a soft-start. UVLO does trigger the soft-start, but without the hiccup timer.

Electrical Characteristics (continued)[17]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_J = -40°C to +125°C with V_{BUS} = 3V to 55V or V_{SYS} = 3V to 55V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V or V_{SYS} = 5V.

Over-Voltage Protection (OVP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{OVP}	Internally Fixed Over-Voltage Protection	V_{BUS} rising threshold, I_{SINK} mode	52	54.2	56.5	V
		V_{SYS} rising threshold, I_{SOURCE} mode	52	54.2	56.5	V
		Hysteresis		2		V
t_{OVP}	OVP Response Time[18]	$V_{BUS} > V_{OVP}$, C_{VSYS} = 10µF, 30A Surge (IEC61000-4-5 8/20 µs) at VBUS		300		ns
t_{OVP_REC}	OVP Recovery Time[19]			$t_{HICCUP}+t_{DEB}+t_R$		ms
V_{OVLO}	Externally Adjustable Over-Voltage Lockout	V_{OVLO} enable threshold	76	96	116	mV
		V_{OVLO} rising OVP threshold	1.12	1.17	1.22	V
		Hysteresis		25		mV
t_{OVLO}	OVLO Response Time[20]	R_L = 100Ω, C_{VSYS} = 10µF		300		ns
t_{OVLO_REC}	OVLO Recovery Time			$t_{HICCUP}+t_{DEB}+t_R$		ms
V_{OVLOS}	Adjustable Over-Voltage Lockout of OVLOS Pin	V_{OVLOS} rising OVP threshold	1.12	1.17	1.22	V
		Hysteresis		25		mV
t_{OVLOS}	OVLOS Response Time[21]	R_L = 100Ω, C_{VSYS} = 0µF		100		ns

Over-Temperature Protection (OTP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{OTP}	IC Junction Over-Temperature Protection	T_J rising threshold		145		°C
		Hysteresis		20		°C
t_{OTP_REC}	OTP Recovery Time			$t_{HICCUP}+t_{DEB}+t_R$		ms

Over-Current Protection (OCP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{OCP}	OCP Current Threshold after t_{LIM_SS}[10]	I_{SINK} mode	15	24		A
		I_{SOURCE} mode	15	24		
t_{OCP}	OCP Response Time[22]			200		ns
t_{OCP_REC}	OCP Recovery Time			$t_{HICCUP}+t_{DEB}+t_R$		ms

17. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.
18. t_{OVP} is time from when the input voltage > V_{OVP} until the output voltage stops rising.
19. t_{OVP_REC} is time from when the input voltage < V_{OVP} until the output voltage reaches 90% of the input voltage.
20. t_{OVLO} is time from when V_{OVLO} rises above its OVP threshold until output voltage stops rising.
21. t_{OVLOS} is time from when V_{OVLOS} rises above its OVP threshold until output voltage starts dropping.
22. t_{OCP} is time from when the switch current > I_{OCP} until switch turns off.

Electrical Characteristics (continued)[23]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation range of T_J = -40°C to +125°C with V_{BUS} = 3V to 55V or V_{SYS} = 3V to 55V. Typical values are specified at T_A = +25°C with V_{BUS} = 5V or V_{SYS} = 5V.

Reverse-Current Protection (RCP) Specifications (KTS1801A only)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{RCP}	RCP Droop Regulation Voltage	I_{SINK}, $V_{RCP} = V_{BUS}–V_{SYS}$, I_{SYS} = 100mA	7	17	27	mV
t_{RCP_REC}	RCP Fast Recovery Time[24]			15		µs

Short-Circuit Protection (SCP) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{HSCP_SS}	Hard Short-Circuit Protection SS Voltage (at 3ms into SS ramp)	I_{SINK} mode, V_{SYS} not rising		1.3		V
		I_{SOURCE} mode, V_{BUS} not rising		1.3		
I_{HSCP}	Hard Short-Circuit Protection Current			I_{OCP}		A
t_{SCP_REC}	SCP Recovery Time		$t_{HICCUP} + t_{DEB} + t_R$			ms

Timing Diagrams

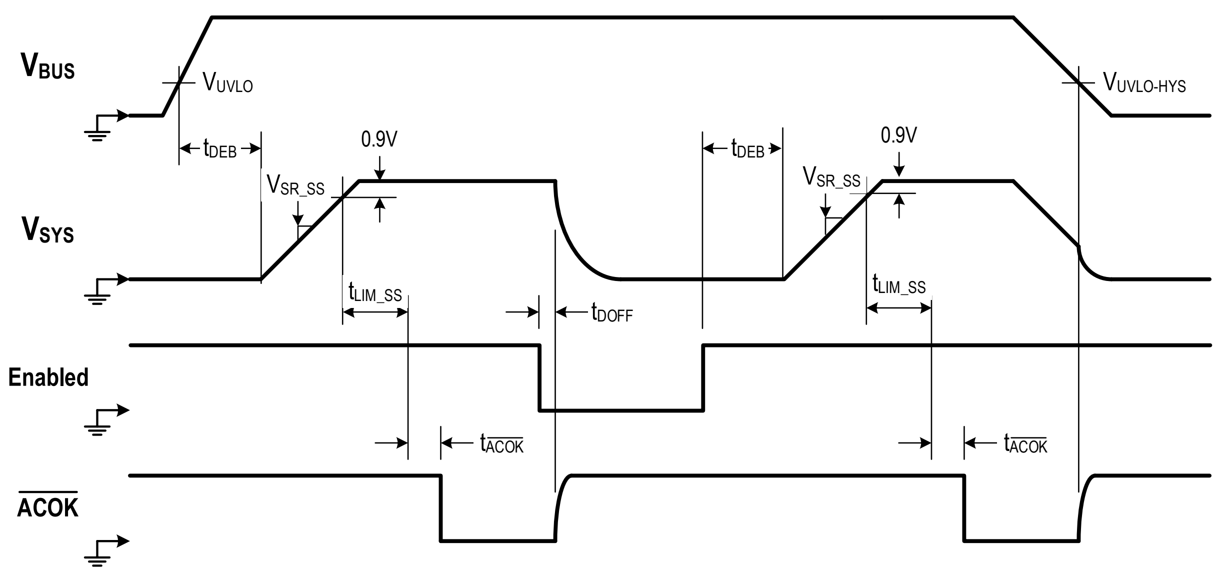


Figure 1. UVLO, Soft-Start and Turn-Off Timing Diagram

23. Device is guaranteed to meet performance specifications over the -40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

24. t_{RCP_REC} is time from when the output voltage falls 140mV below the input voltage until switch turns back on. Before measuring, first raise the output voltage significantly above the input voltage.

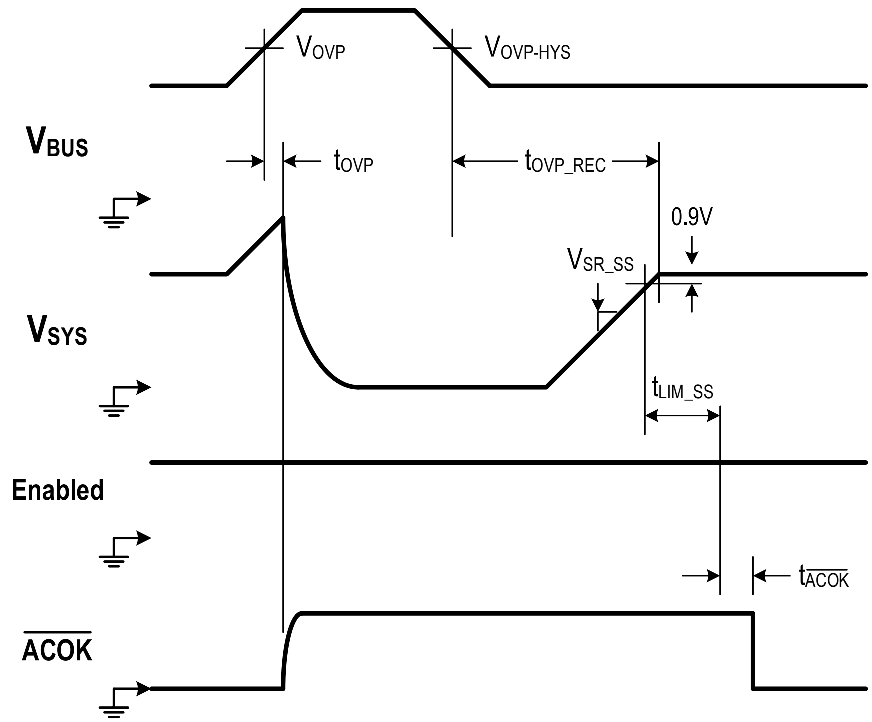


Figure 2. OVP Timing Diagram (OVLO

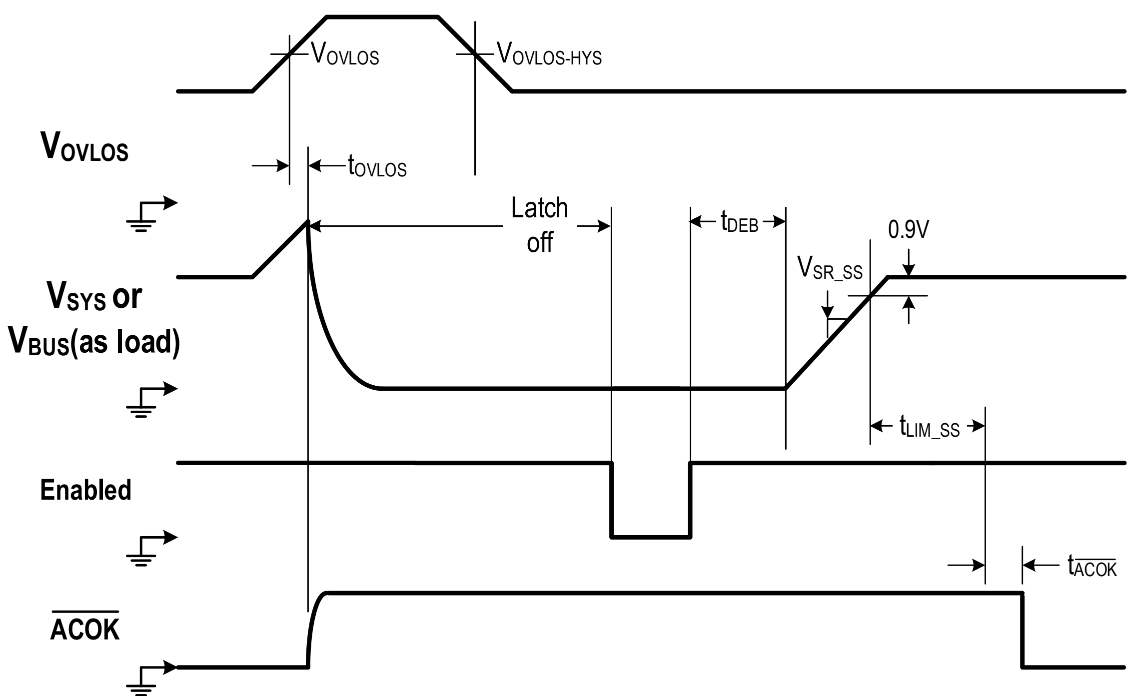


Figure 3. OVP Timing Diagram (OVLOS pin)

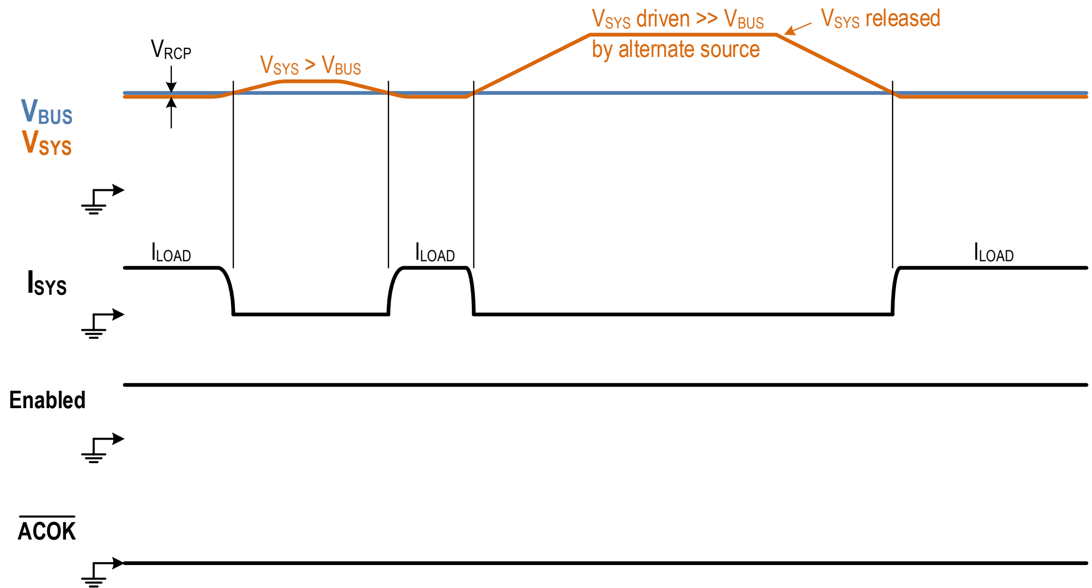


Figure 4. "Ideal Diode" RCP Timing Diagram (KTS1801A only)

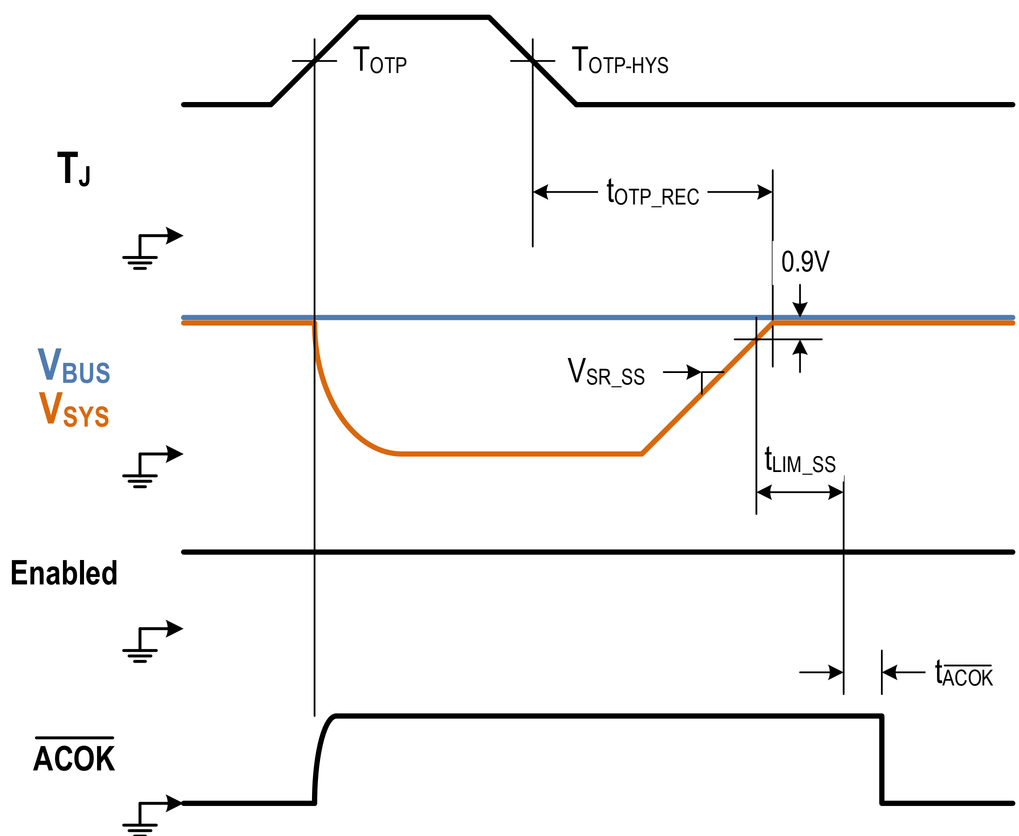


Figure 5. OTP Timing Diagram

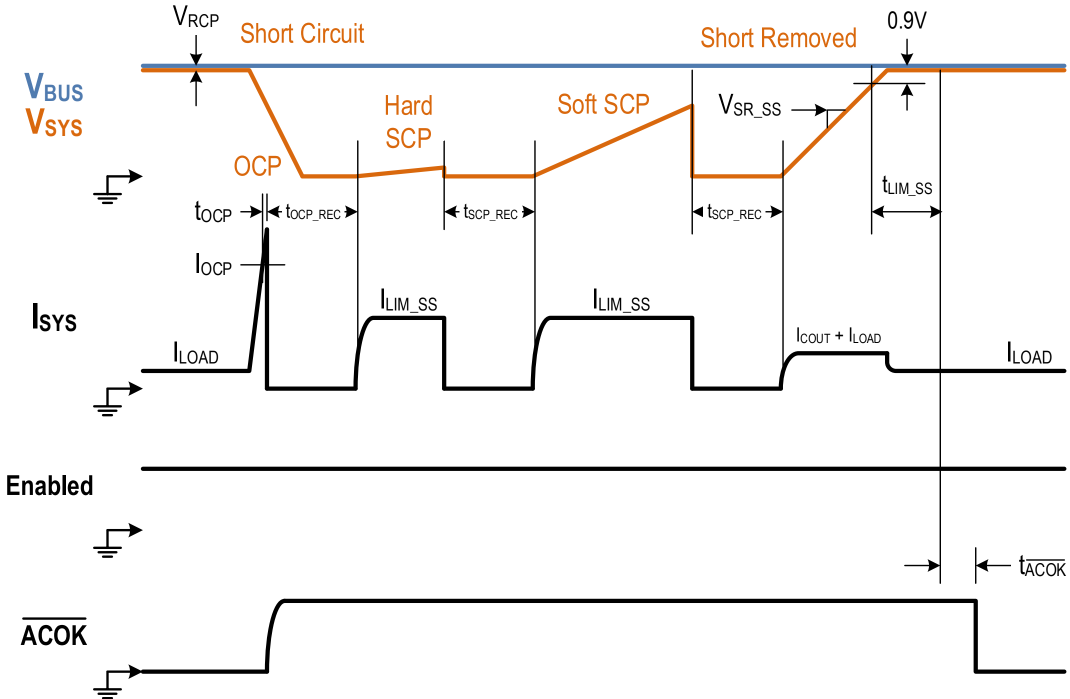


Figure 6. OCP and SCP Timing Diagram

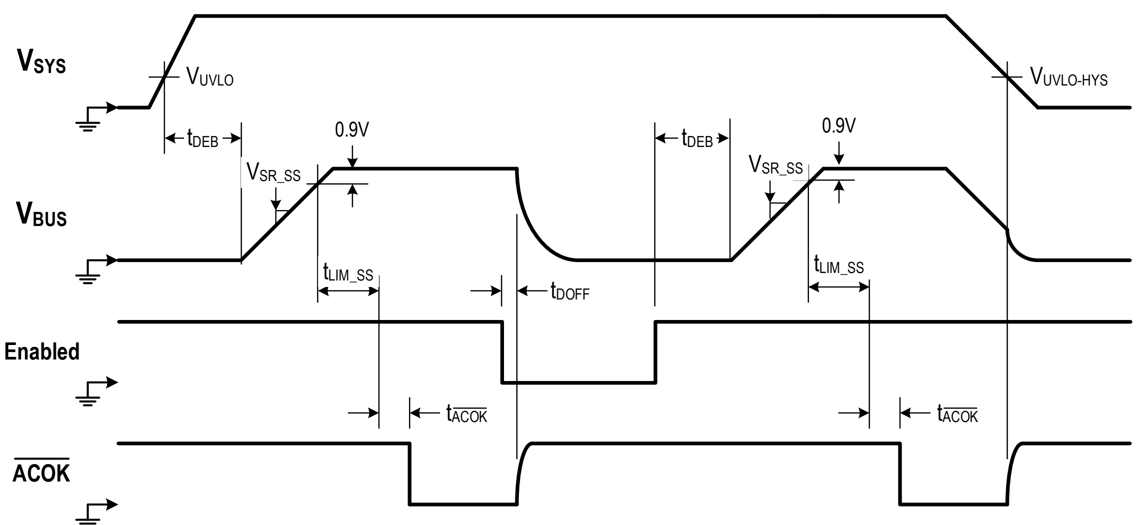
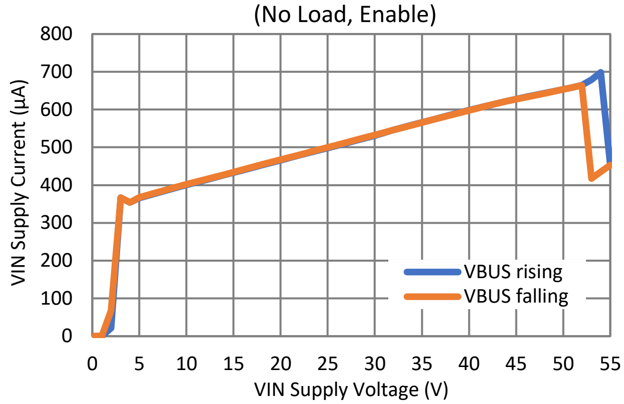


Figure 7. UVLO, Soft-Start and Turn-Off Timing Diagram in I_{SOURCE} Mode (KTS1801B Only)

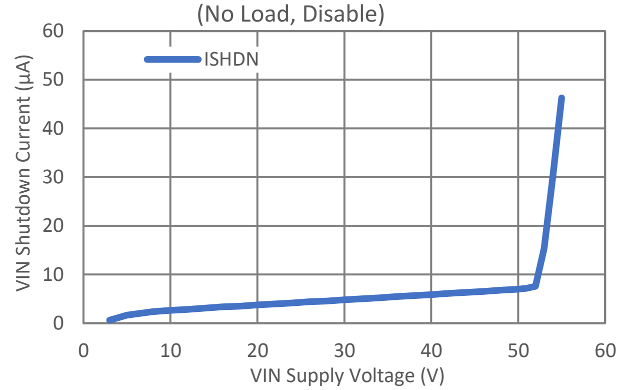
Typical Characteristics

C_{VBUS} = 10µF, C_{SYS} = 4x 10µF, and T_A = +25°C unless otherwise noted.

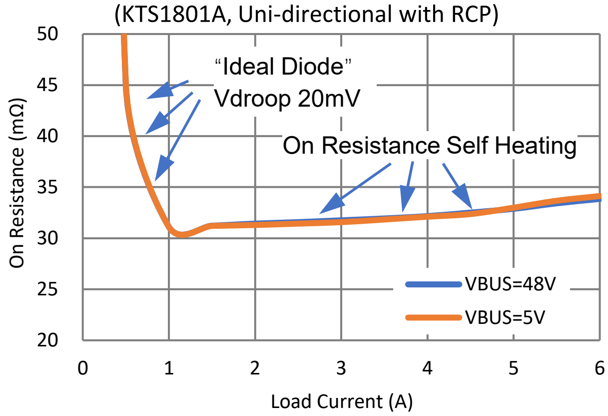
VBUS Supply Current Vs. Supply Voltage
(No Load, Enable)



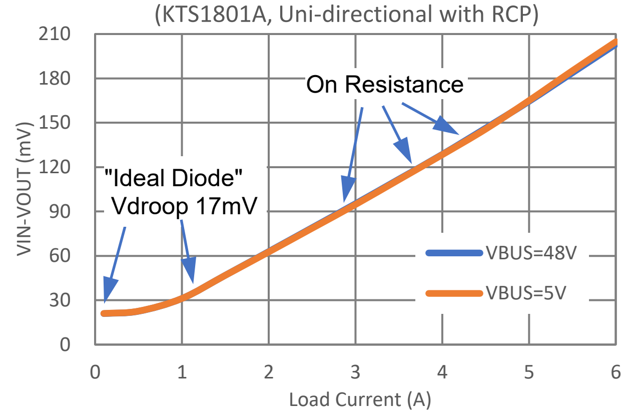
VBUS Shutdown Current Vs. Supply Voltage
(No Load, Disable)



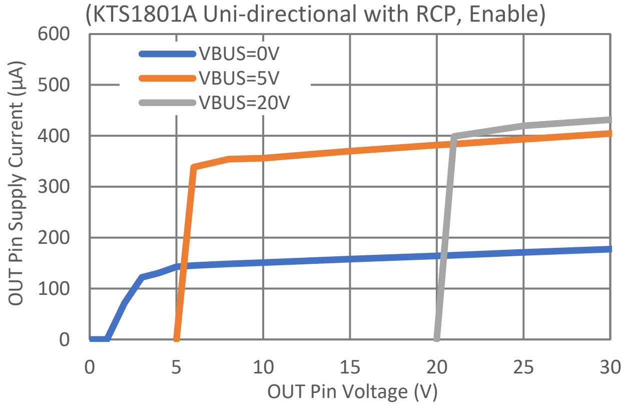
On Resistance Vs. Load Current
(KTS1801A, Uni-directional with RCP)



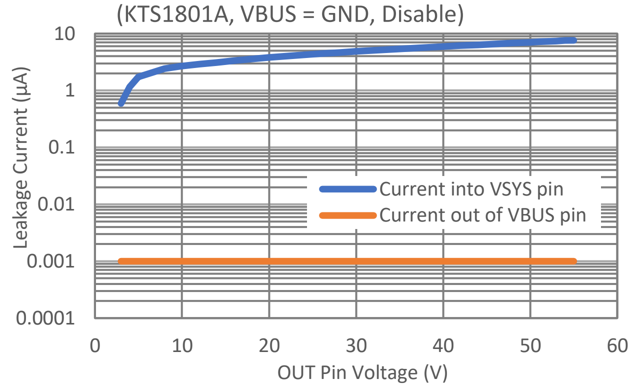
"Ideal Diode" Vdroop Vs. Load Current
(KTS1801A, Uni-directional with RCP)



RCP Supply Current at VSYS Pin
(KTS1801A Uni-directional with RCP, Enable)



Reverse Leakage Current at VSYS and VBUS Pins
(KTS1801A, VBUS = GND, Disable)

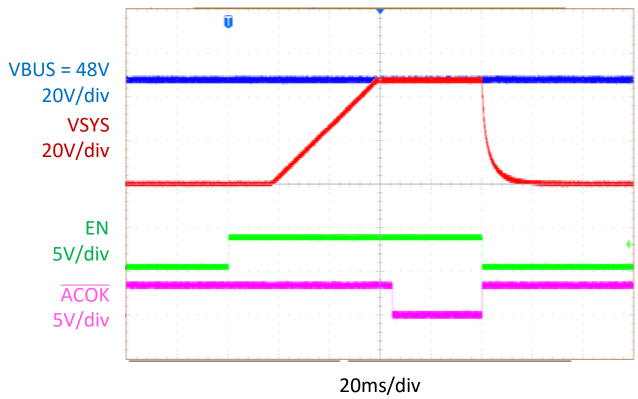


(continued next page)

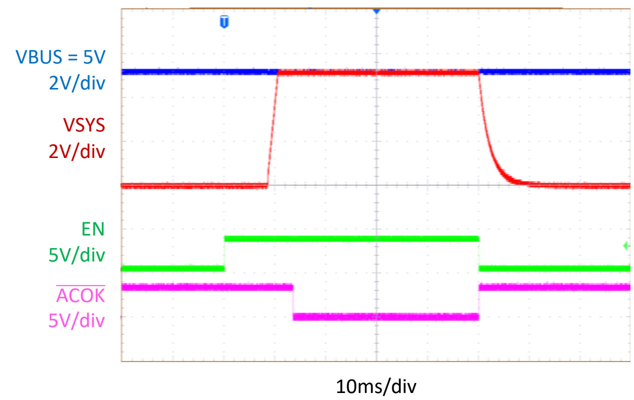
Typical Characteristics

C_{VBUS} = 10µF, C_{SYS} = 4x 10µF, and T_A = +25°C unless otherwise noted.

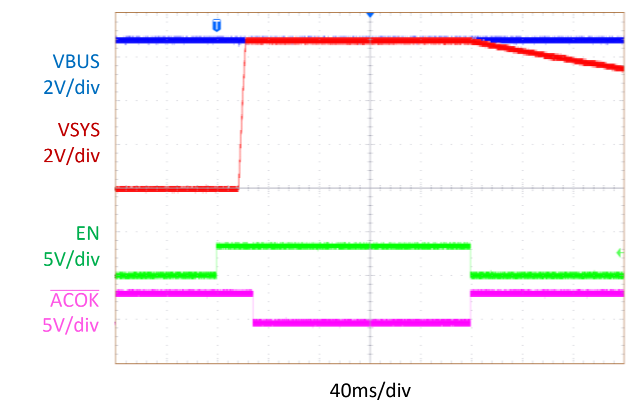
Enable, Soft-Start, Shutdown Response
(VBUS = 48V, RLoad = 100Ω, Isink Mode)



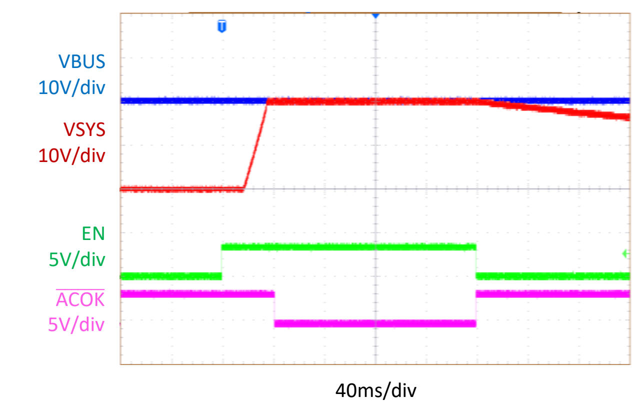
Enable, Soft-Start, Shutdown Response
(VBUS = 5V, RLoad = 100Ω, Isink Mode)



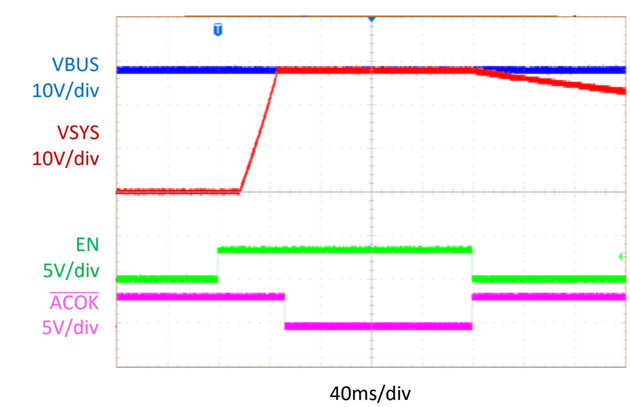
Soft-Start into Big Cap at VBUS = 5V
(CBUS = 10µF, C_{VSYS} = 2000µF + 4x10µF, R_{Load}_VSYS = 400Ω)



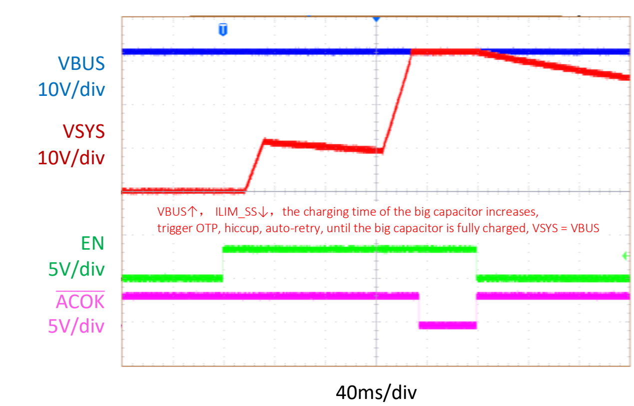
Soft-Start into Big Cap at VBUS = 20V
(CBUS = 10µF, C_{VSYS} = 2000µF + 4x10µF, R_{Load}_VSYS = 400Ω)



Soft-Start into Big Cap at VBUS = 28V
(CBUS = 10µF, C_{VSYS} = 2000µF + 4x10µF, R_{Load}_VSYS = 400Ω)



Soft-Start into Big Cap at VBUS = 32V
(CBUS = 10µF, C_{VSYS} = 2000µF + 4x10µF, R_{Load}_VSYS = 400Ω)



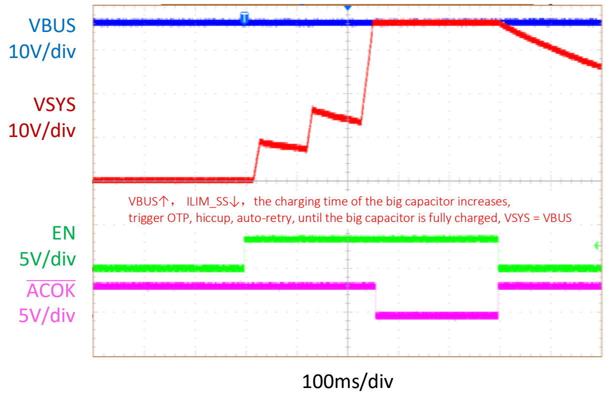
(continued next page)

Typical Characteristics

C_{VBUS} = 10µF, C_{SYS} = 4x 10µF, and T_A = +25°C unless otherwise noted.

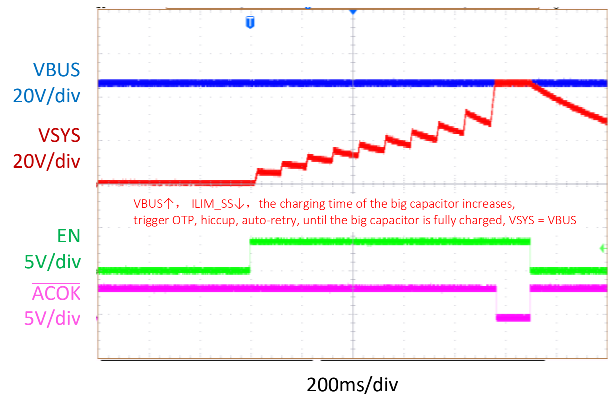
Soft-Start into Big Cap at VBUS = 36V

(CBUS = 10µF, C_{VSYS} = 2000µF + 4x10µF, R_{Load}_VSYS = 400Ω)



Soft-Start into Big Cap at VBUS = 48V

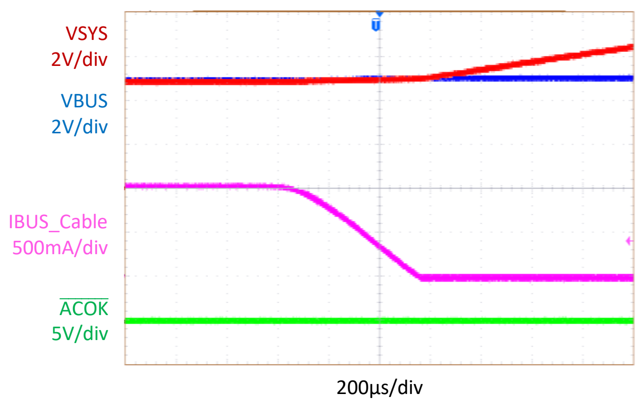
(CBUS = 10µF, C_{VSYS} = 2000µF + 4x10µF, R_{Load}_VSYS = 400Ω)



RCP Response

KTS1801A Uni-directional with RCP

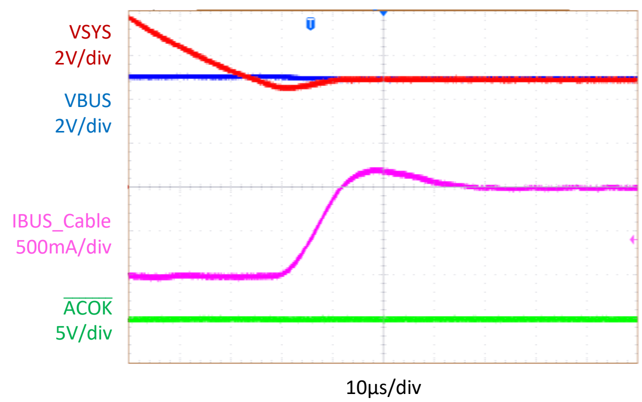
(VBUS = 5.1V, R_{CABLE} = 200mΩ, Load = 5Ω, VSYS = 5V → 9V)



RCP Fast Recovery

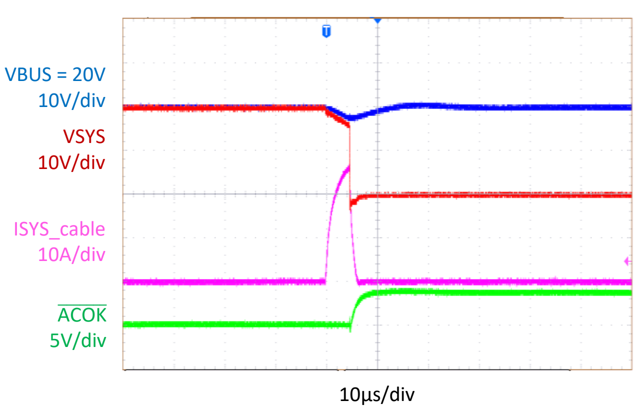
KTS1801A Uni-directional with RCP

(VBUS = 5.1V, R_{CABLE} = 200mΩ, Load = 5Ω, VSYS = 9V → 5V)



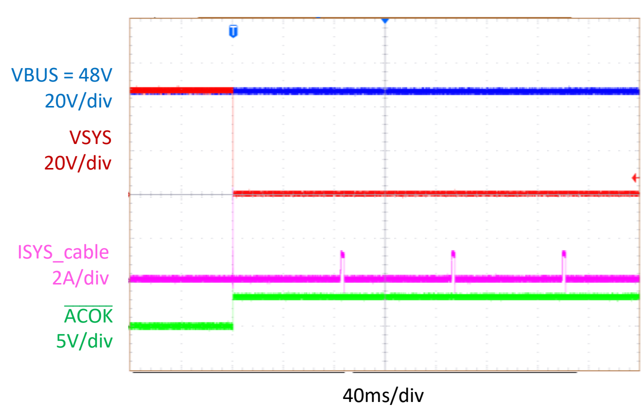
OCP Response

(VBUS = 20V, VSYS = 20V → Short Circuit)



SCP Response with Auto - Retry

(VBUS = 48V, VSYS = 48V → Short Circuit)



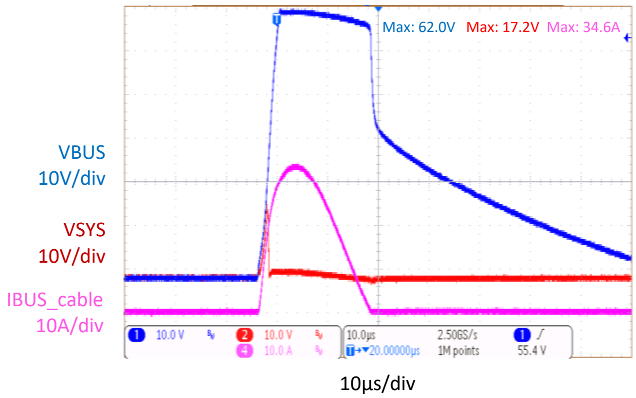
(continued next page)

Typical Characteristics

C_{VBUS} = 10µF, C_{SYS} = 4x 10µF, and T_A = +25°C unless otherwise noted.

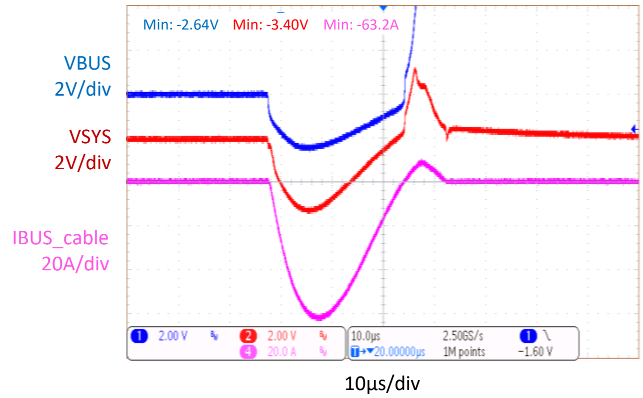
Surge Transient Response

(VBUS = 0V + 130V Surge Voltage)



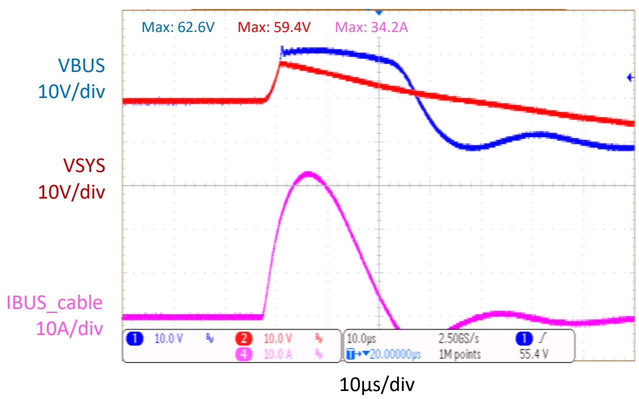
Surge Transient Response

(VBUS = 0V - 130V Surge Voltage)



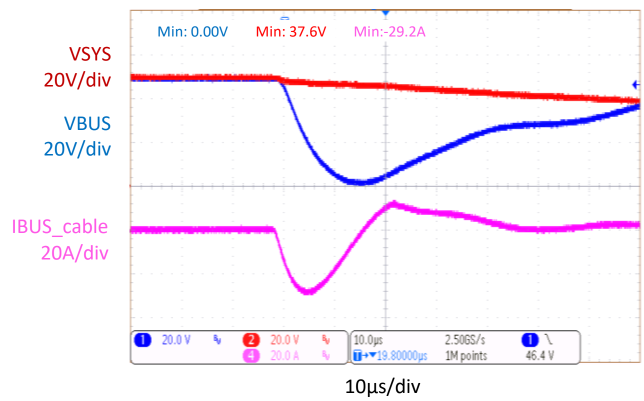
Surge Transient Response

(VBUS = 48V + 80V Surge Voltage, R_{Load} = 100Ω)



Surge Transient Response

(VBUS = 48V - 80V Surge Voltage, R_{Load} = 100Ω)



Functional Block Diagram

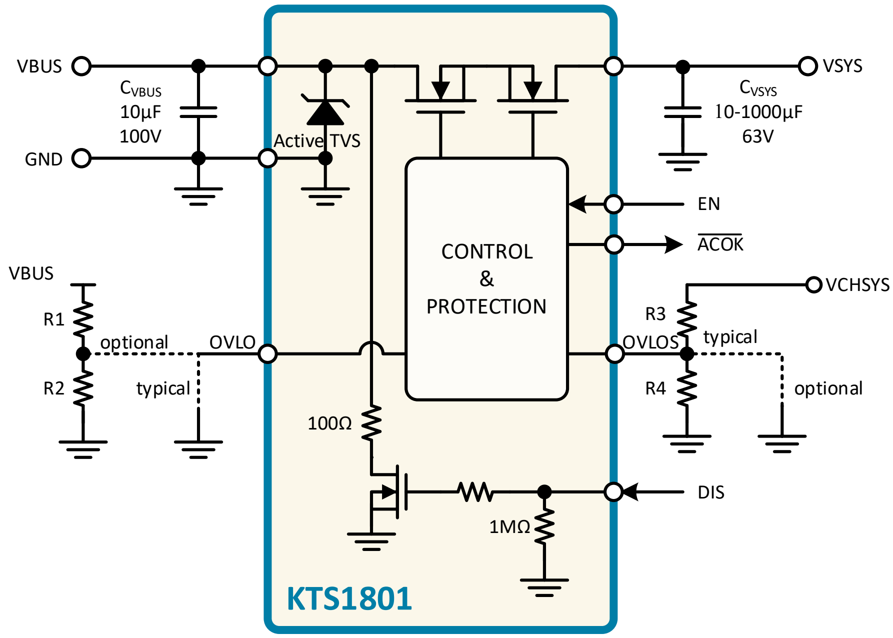


Figure 8. Functional Block Diagram

Functional Description

The KTS1801 is a slew-rate controlled, 31mΩ (typ) low resistance MOSFET load switch intended to be inserted between a power source and a load to isolate and protect against abnormal voltage and current conditions. Featuring slew-rate controlled soft-start and soft-start current limit to prevent excessive large inrush current, the KTS1801 also features several additional protection functions. These include input under-voltage lockout protection, input over-voltage protection, output short-circuit protection, over-current protection, over-temperature protection, and input transient voltage suppression for ±130V surge and ±30kV ESD protections. The KTS1801A switch also acts as a "ideal diode" reverse-current protection with V_F = 17mV and 15µs fast recovery to ensure current flows in only the intended sink direction.

Operating from a wide input voltage range of 3V to 55V, the KTS1801A is optimized for USB Type-C Power Delivery (PD) current-sink applications up to 48V extended power range (EPR) that require essential protection and enhanced system reliability. While in the OFF state, the KTS1801A blocks voltages of up to 56V on the VBUS and VSYS pins and prevents current flow. While in the ON state, the KTS1801A withstands voltages of up to 56V on the VBUS and VSYS pins, passes valid input voltages and current from VBUS to VSYS, and blocks reverse current from VSYS to VBUS. Due to the ideal-diode behavior, two or more KTS1801A parts can be used in parallel to support systems that benefit from "diode-OR" power routing.

KTS1801A has automatic reverse-current protection (RCP) feature which acts as an "ideal diode" with fast recovery and isolates VBUS when charging or powering the system via another port. KTS1801B supports bi-directional mode when enabled so it is optimized for USB Type-C Power Delivery (PD) current-sink and/or current-source applications.

Shutdown and Enable

The KTS1801 has EN active-high input logic. When disabled, the main power MOSFETs are turned off, and the device enters low-power shutdown mode. When enabled, all additional protection circuits are active, and if no fault condition exists, the main power MOSFETs are turned ON.

Under-Voltage Lockout (UVLO)

When $V_{BUS} < V_{UVLO}$ in I_{SINK} mode or $V_{SYS} < V_{UVLO}$ in I_{SOURCE} mode, the power switch is disabled. Once V_{BUS} or V_{SYS}, respectively, exceeds V_{UVLO}, the power switch is controlled by the enable pins and fault detection circuits.

Soft-Start (SS)

The internal soft-start function allows the KTS1801 to charge a total output capacitance of 1000µF to 5V without excessive in-rush current. Soft-start controls the output voltage ramp slew-rate at 1V/ms. Use the below formula to calculate the current required to charge a combination of load current and output capacitance:

$$I_{IN\_SS} = I_{LOAD} + C_{OUT}(1V/ms)$$

Note that in addition to the soft-start voltage ramp, a simultaneous soft-start current limit of 2A prevents excessive heat when entering into an output short-circuit or a large total output capacitance conditions. This current limit turns off 2ms after the output voltage ramp exceeds the input voltage minus 0.9V, regardless of whether the output voltage is following the slew rate or limited by the soft-start current limit. After an additional 2ms delay, the $\overline{\text{ACOK}}$ flag indicates a power good condition. See the *Heavy Load Soft-Start Response* in the *Typical Characteristics* section.

Over-Voltage Protection (OVP) of OVLO pin

Once enabled, if the input voltage exceeds the V_{OVP} threshold, the power switch is disabled due to an OVP fault. Once the input voltage drops below V_{OVP} (and no other fault is detected and the device is still logically enabled via EN), the power switch is re-enabled after the hiccup timer, soft-start debounce and soft-start ramp time.

The OVLO pin is used to adjust the over-voltage threshold externally. The default internal over-voltage threshold is 54.2V when the OVLO pin is tied to GND. Biasing the OVLO pin with a resistive voltage divider adjusts the over voltage threshold from 4V to 55V as in the below formula:

$$V_{OVP} = V_{OVLO}\left(1 + \frac{R1}{R2}\right)$$

where V_{OVLO} = 1.17V. Connect R1 from VBUS to OVLO. Connect R2 from OVLO to ground. For dedicated current source applications, it is optional to connect the resistive voltage divider to VBUS or VSYS, depending upon the needs of the application.

Over-Voltage Protection (OVP) and latch off of OVLOS pin

When EN = H, the switch is logically enabled. However, if the system voltage after the charger exceeds the over-voltage threshold V_{OVPS}, the power switch is disabled due to an OVP fault and it will ***latch off***. When KTS1801 is latched off, the EN input pin when toggled (from High to Low to High) allows to restart the device after OVLOS OVP fault latch. See Figure 3.

The OVLOS pin is used to adjust the over-voltage threshold for the system power rail after the charger. Biasing the OVLOS pin with a resistive voltage divider adjusts the over-voltage threshold from 4V to 55V as in the below formula:

$$V_{OVPS} = V_{OVLOS}\left(1 + \frac{R3}{R4}\right)$$

where V_{OVLOS} = 1.17V. Connect R3 from VCHSYS to OVLOS. Connect R4 from OVLOS to ground. See Figure 8. Connect OVLOS pin to GND if it is not used.

Over-Current Protection (OCP)

The KTS1801 includes output over-current protection (OCP) that protects the IC from damage when an excessive over-current or short-circuit event suddenly appears. The OCP threshold is purposely high above the rated current for the KTS1801 such that system load-pulses do not easily trigger OCP. The OCP circuit disables the power switch, so the current becomes zero. After an OCP event (and no other fault is detected and the device is still logically enabled via EN), the power switch is re-enabled after the hiccup timer, soft-start debounce and soft-start ramp time.

Short-Circuit Protection (SCP)

The KTS1801 includes output short-circuit protection (SCP). In virtually all conditions, the KTS1801 remains undamaged during continuous SCP events.

If an SCP event occurs while the KTS1801 is already enabled and working, OCP is the first line of defense and responds very quickly. In this case, the current from the input capacitor through the switch to the output increases very rapidly as soon as the output voltage begins to collapse. The OCP threshold is purposely high above the rated current for the KTS1801 such that system load-pulses do not easily trigger OCP.

In addition, if the output voltage collapses to less than 50% without reaching OCP, such as during a soft short-circuit event, an SCP fault is triggered, causing the switch to open and triggering a hiccup and auto-retry sequence.

In case of auto-retry (after the hiccup timer) or simply starting into a pre-existing SCP condition, the KTS1801 furthermore includes SCP detection during soft-start if the output voltage is not ramping up. SCP checks if the output voltage has risen to more than 1.3V at 3ms into the soft-start ramp. If not, the KTS1801 terminates soft-start, turns off the switch, and will auto-retry after the hiccup timer. The $\overline{\text{ACOK}}$ flag remains high until a successful soft-start is completed.

"Ideal Diode" Reverse-Current Protection (RCP, KTS1801A only)

The KTS1801A offers reverse-current protection regardless of the enable logic level. When disabled, all current flow is blocked. When enabled, the RCP acts as a voltage droop regulator. Once the voltage on V_{SYS} is higher than V_{BUS} minus 17mV, the RCP circuit reduces the MOSFET gate drive to try and maintain the regulated 17mV droop, thereby acting as an "ideal diode" with Vf = 17mV. See Figure 9.

This control method blocks all reverse current within the RCP control loop bandwidth. During recovery, RCP includes a 15µs fast recovery circuit whenever the output falls again below the input voltage. Note that RCP is not defined as a fault condition and has fast recovery without initiating the hiccup and auto-retry sequence.

The RCP circuit makes it possible to connect two or more USB charging ports to a single charger input in a "diode-OR" configuration with autonomous reverse-current blocking.

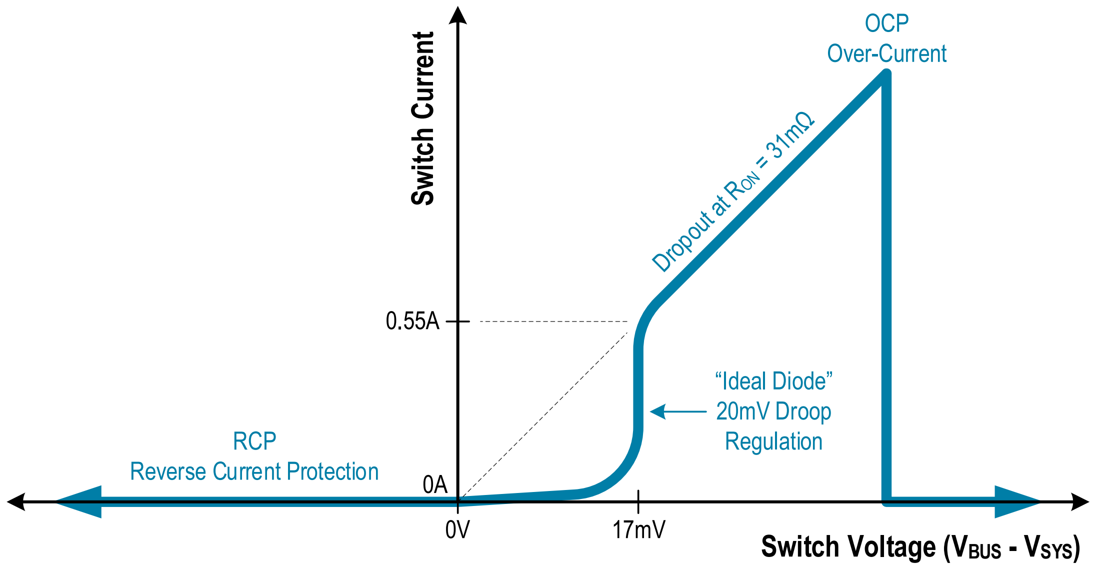


Figure 9. "Ideal Diode" Reverse-Current Protection V-I Curve

Over-Temperature Protection (OTP)

When device junction temperature exceeds 145°C, the OTP circuit disables the power switch. Once the device junction temperature decreases below 130°C (and no other fault is detected and the device is still logically enabled via EN), the power switch is re-enabled after the hiccup timer, soft-start debounce and soft-start ramp time.

Transient Voltage Suppression (TVS)

The KTS1801 integrates an active clamp transient voltage suppressor (TVS) from VBUS to GND. The integrated TVS circuit and fast OVP switch work as an optimized system to protect the KTS1801 and downstream circuits for IEC surge and ESD events. The TVS protection is always active, whether the KTS1801 is in shutdown or enable mode.

$\overline{\text{ACOK}}$ Output Flag

The $\overline{\text{ACOK}}$ output is an open-drain output that requires an external pull-up resistor with recommended value in the 10kΩ to 200kΩ range. The $\overline{\text{ACOK}}$ pin indicates the fault status. When there is no fault (UVLO, OVP, OCP, SCP, and OTP are not triggered) and the power switch is ON, then the $\overline{\text{ACOK}}$ flag is pulled low to indicate the power is good. Otherwise, the $\overline{\text{ACOK}}$ flag is high impedance.

Auto-Retry with Hiccup Timer

For fault conditions that cause the switch to open, the KTS1801 automatically restarts via the hiccup timer and soft-start sequence once the fault is removed. If any fault or the same fault is detected again, the switch opens again, and auto-retry repeats. This continues until the fault is removed (normal operation) or the device is shutdown via EN or input power is removed (UVLO). Note that RCP event is not defined as fault condition and has fast recovery without initiating the auto-retry sequence.

VBUS Active Discharge (DIS)

The KTS1801 includes an active discharge circuit to pull VBUS below to vSafe0V within USB Type-C compliant discharge timing specifications. The pull-down resistance depends upon the DIS pin voltage level. See the *DIS*

Specifications section of the *Electrical Characteristics* table. As shown in Figure 8, the DIS circuit operation is fully independent of the rest of the IC and does NOT depend upon chip being powered or the EN status.

Applications Information

External Component Selection

VBUS Capacitor C_{VBUS}

For most applications, connect a 1µF to 10µF ceramic capacitor as close as possible to the device from VBUS to GND to minimize the effect of parasitic trace inductance. 100V rated capacitors with X5R or better dielectric are recommended. For optimal surge and ESD performance, 10µF is preferred.

VSYS Capacitor C_{VSYS}

For most applications, connect from 10µF to 1000µF total capacitance from VSYS to GND. Typical applications use 30µF to 100µF as needed for system load-transients. At minimum, connect a 10µF ceramic capacitor as close as possible to the device to minimize the effect of parasitic trace inductance. 63V or 100V rated capacitors with X5R or better dielectric are recommended. Lower voltage ratings may be acceptable when using the OVLO pin to set a lower over-voltage protection threshold. For bulk capacitance, add ceramic, polymer or other capacitor technologies in parallel as needed to meet the needs of the application.

Recommended PCB Layout

Good PCB thermal design is required to support heavy load currents. The KTS1801 EVB is designed with similar layout as Figure 10, but it extends the fill area for the VSYS, VBUS, and GND copper planes for increased thermal performance. Due to the number of bumps on VSYS and VBUS, these two planes are especially important for heat dissipation and should not be ignored. Adding back-side and/or buried-layer fill area with thermal vias helps significantly. The WLCSP package has very low Theta-JC, which is ideal when using thermally conductive material laid over the IC, external components, and PCB. With good thermal design, applications up to 6.5A continuous may be supported.

The PCB layout for the KTS1801 is quite simple. Place the VSYS and VBUS capacitors near the IC. Connect the capacitor ground terminals together and to the GND pins using the top-side copper. Route the control signals on buried layers. With 0.5mm bump pitch, signal traces may be routed between bumps to reach inner bumps. Or route the inner bumps using filled, in-pad vias, as these have become more available even in low-cost PCB manufacturing. As an example, the KTS1801 EVB uses filled, in-pad vias. Depending upon the application's needs, connect any unused control pins (OVLO, OVLOS, $\overline{\text{ACOK}}$, and/or DIS) to ground. Do not ground the G1(NC) pin if co-layout KTS1801 with KTS1800 is required.

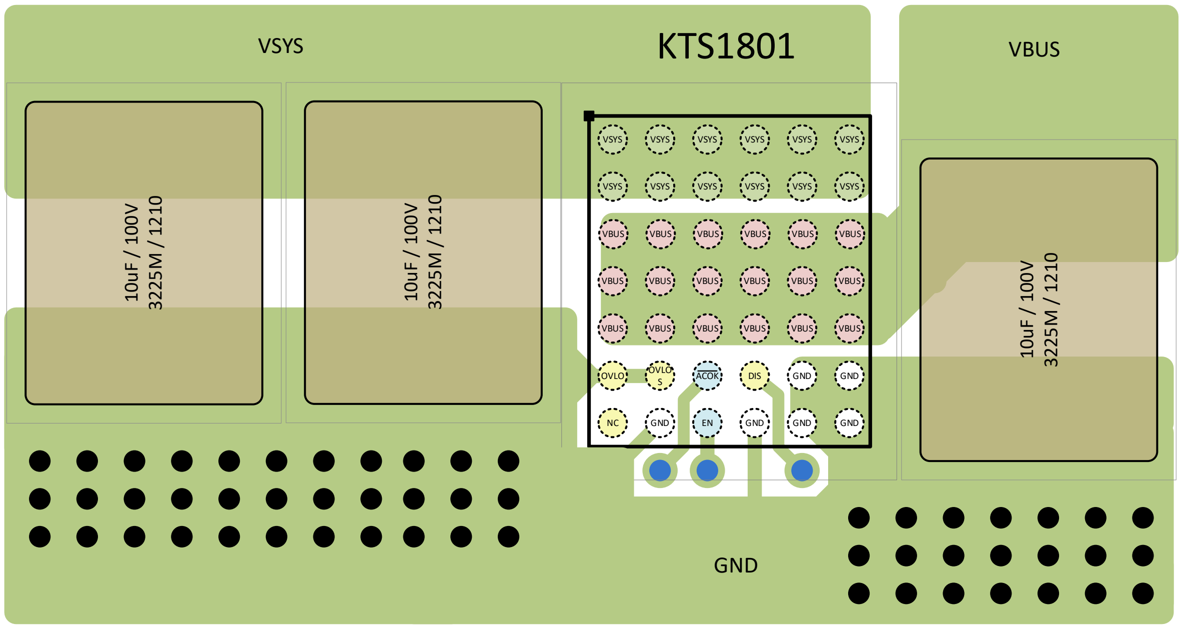


Figure 10. Recommended PCB Layout

Safe Operating Area (SOA)

See Figure 11 and Figure **12** for the SOA of the KTS1801. SOA curves are normally associated with discrete MOSFETs (which are sometimes co-package with a controller IC). In these competing systems, precautions are necessary to stay within the SOA area. However, the KTS1801 is a monolithic IC with integrated protection features to *automatically* keep its operation within the SOA area. For example, it includes over-voltage protection (OVP) and over-current protection (OCP) with very fast response times. It also includes over-temperature protection (OTP) that is measured on the same monolithic die as the integrated power MOSFETs. Additionally, soft-start is controlled with a voltage ramp and current limit protection (Soft-Start CLP) to safely soft-start even in systems with very high capacitance at the output. Furthermore, the integrated TVS and back-to-back MOSFET switch are optimized to work together as a system, including their tolerances over temperature and process corners.

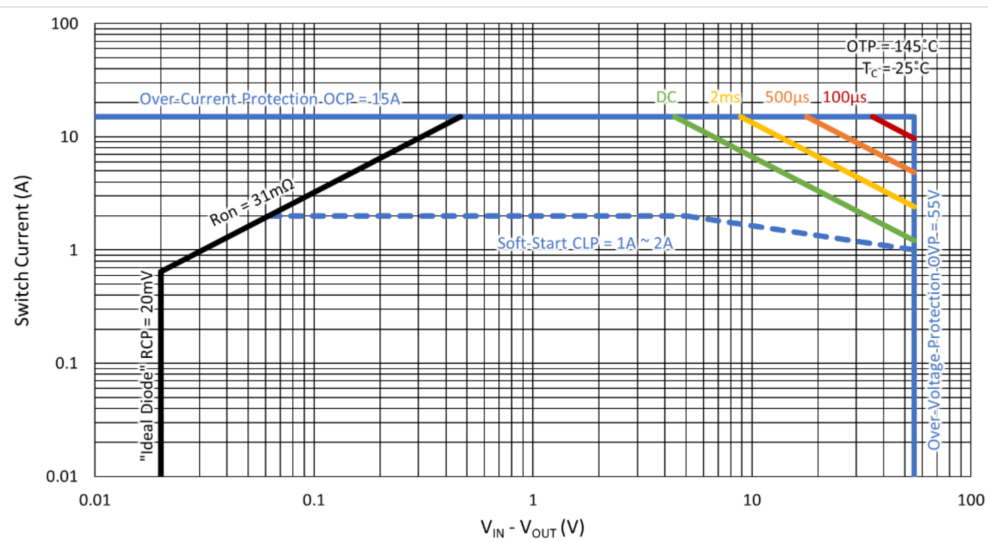


Figure 11. Safe Operating Area (SOA) for T_C = 25℃

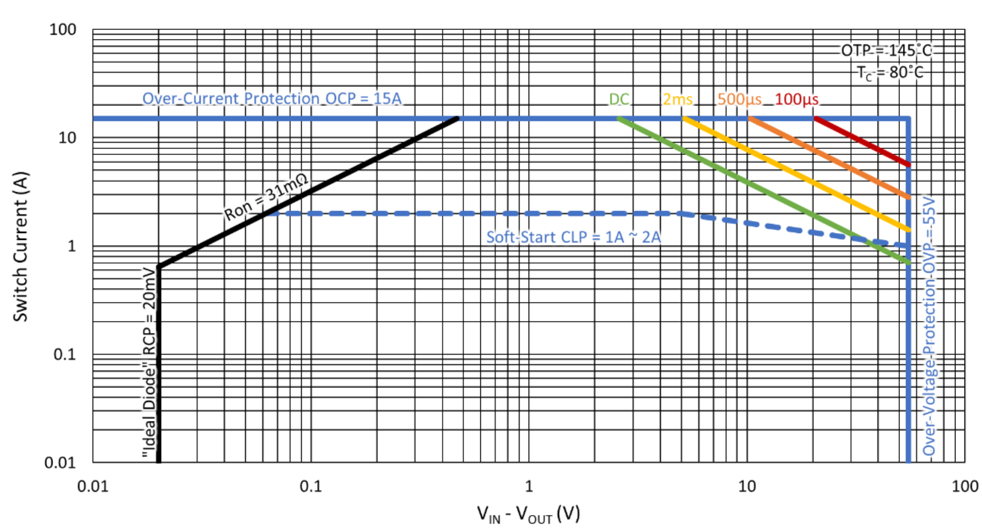
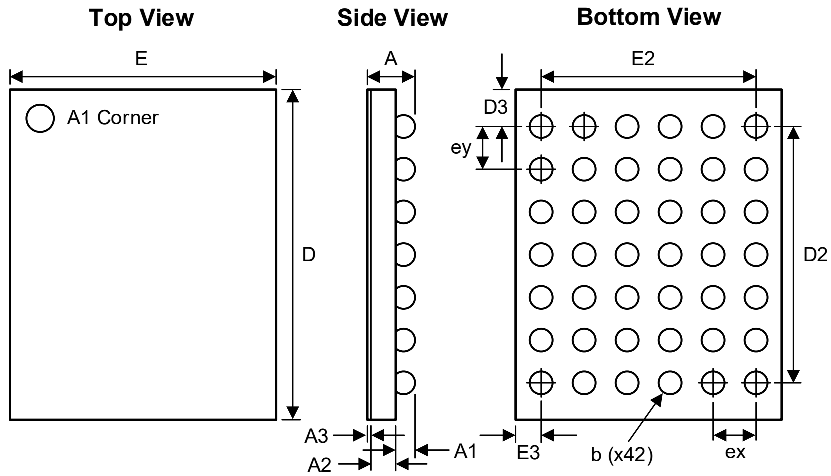


Figure 12. Safe Operating Area (SOA) for T_C = 80℃

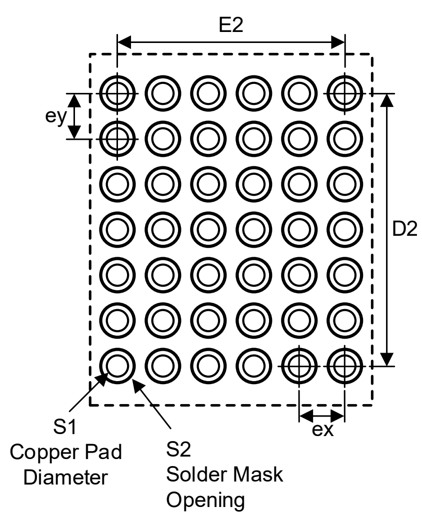
Packaging Information

WLCSP76-42 (3.865mm x 3.095mm x 0.555mm)



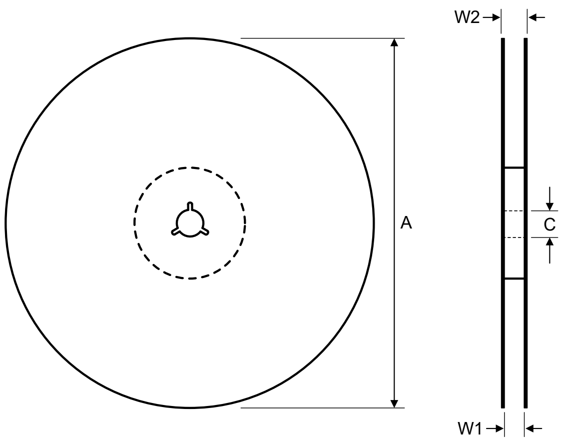
Dimension	mm		
	Min.	Typ.	Max.
A	0.517	0.555	0.592
A1	0.204	0.224	0.244
A2	0.293	0.306	0.318
A3	0.020	0.025	0.030
b	0.248	0.268	0.288
D	3.815	3.865	3.915
D2	3.000 REF.		
D3	0.433 REF.		
E	3.045	3.095	3.145
E2	2.500 REF.		
E3	0.298 REF.		
ex	0.500 REF.		
ey	0.500 REF.		
S1	–	0.20	–
S2	–	0.30	–

Recommended Footprint



Packing Material Information

Reel Dimensions



Dimension	mm		
	Min.	Typ.	Max.
A	176	178	181
C	12.8	13.0	13.5
W1	12.4	12.4	14.4
W2	—	—	18.4

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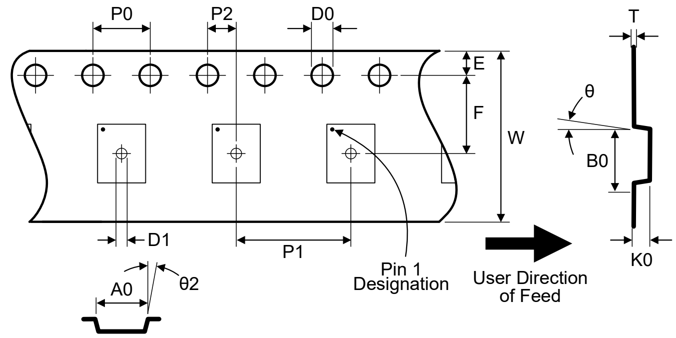
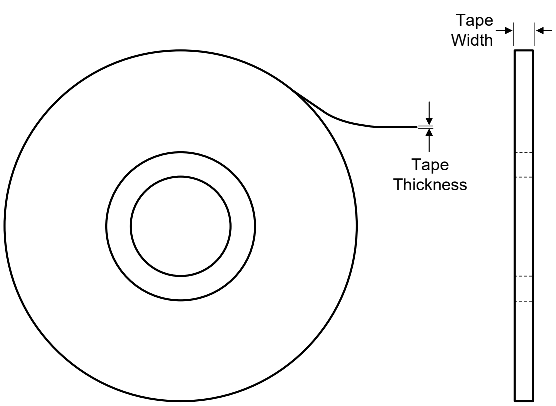
Carrier Tape Dimensions



Dimension	mm		
	Min.	Typ.	Max.
A0	3.30	3.35	3.40
B0	4.07	4.12	4.17
K0	0.71	0.76	0.81
P0	3.9	4	4.1
P1	7.9	8	8.1
P2	1.95	2.00	2.05
D0	1.50	1.50	1.60
D1	0.70	0.75	0.80
E	1.65	1.75	1.85
F	5.45	5.50	5.55
10P0	39.8	40	40.2
W	11.90	12.00	12.30
T	0.20	0.25	0.30
ϴ			5°
ϴ2			5°

RND-DPK-0711 01

Cover Tape Dimensions



Dimensions	Dimension	mm		
		Min.	Typ.	Max.
	Tape Thickness	0.04	0.05	0.06
12mm	Tape Width	9.2	—	9.6

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