15W Flyback Regulator with Digital Isolator Integrated Feedback

Features

- Wide V_{IN} Range: 7V to 100V
- Integrated 1.5A, 150V Power MOSFET Switch
- 430mΩ (typ.) on-resistance of MOSFET Switch
- Integrated Feedback and Digital Isolator
- Internal Startup Regulator
- ±1.5% Feedback Voltage Reference
- 3kV-rms Isolation
- Frequency Adjustable from 100kHz to 1MHz
- Adjustable Soft-Start Time
- Precision Enable for Adjustable UVLO
- Optional Primary Side Bias for Optimized Efficiency
- Integrated Cycle-by-Cycle Current Limit, Input UVLO, Over Current Protection, Short-Circuit Protection, and Thermal Shutdown Protection
- SOIC-16 Wide Body (10.3mm x 7.5mm)
- -40°C to 125°C Operating Junction Temperature Range
- Safety Certification: UL1577 (No. E517623)

Brief Description

The KTB1100 is a highly integrated isolated flyback regulator with integrated power MOSFET switch, internal feedback, and integrated digital isolator. The internal digital isolated eliminates the need to use an external optocoupler and enables small total solution size. The device operates over a wide input voltage range from 7V to 100V to support a variety of applications.

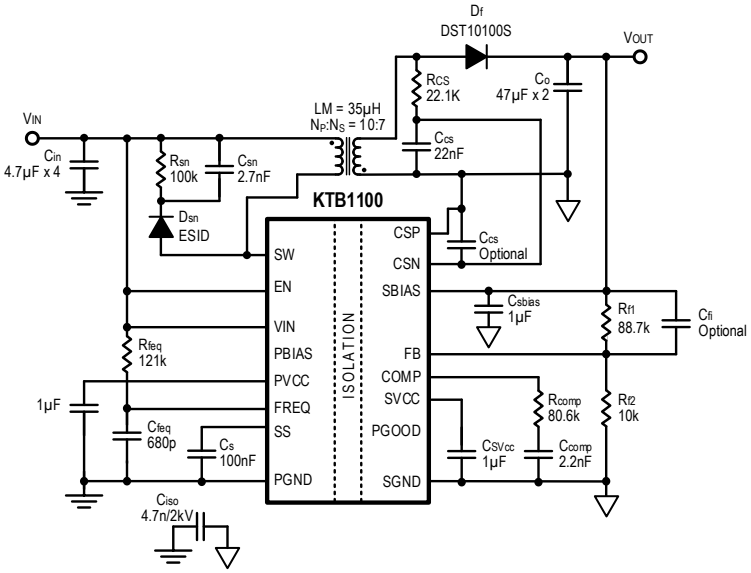
The KTB1100 employs current-mode constant on-time (COT) control for fast transient response as well as superior output voltage regulation. The device features an adjustable soft-start function to limit inrush current during start-up. The device has integrated protection features including input voltage UVLO, output overvoltage protection (OVP), cycle-by-cycle current limit, short-circuit protection and thermal shutdown.

The KTB1100 is available in RoHS and Green compliant SOIC-16 package.

Applications

- Battery Management System (BMS) in EVs
- Telecom and Communications Power Systems
- Industrial PLCs, Smart Meters
- Power-Over-Ethernet (PoE)
- Bias supply for isolated DC-DC converters
- Low power isolated power modules

Typical Application

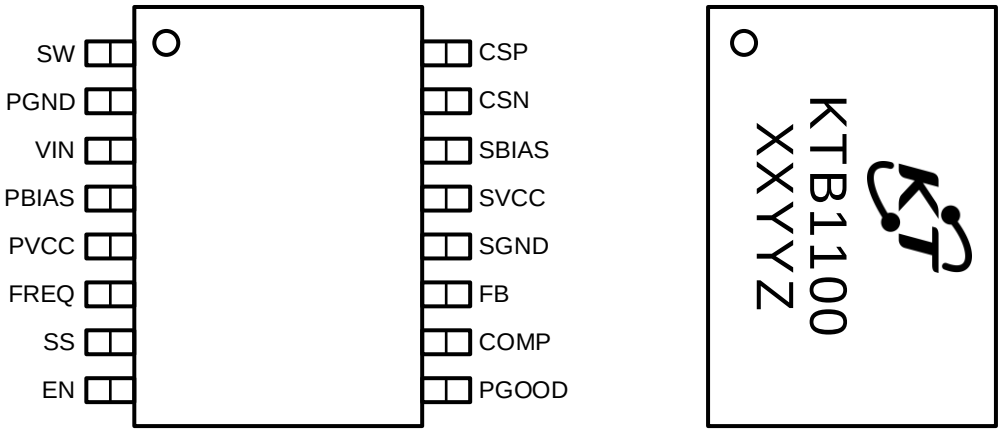


Pin Descriptions

Pin #	Name	Function
1	SW	Drain of Internal Power MOSFET.
2	PGND	Primary Side Ground.
3	VIN	Input supply voltage with 7V to 100V operating range.
4	PBIAS	Optional input to primary side PVCC bias regulator. Powering PVCC from an external supply instead of VIN can reduce power loss at high VIN. For PBIAS > 8V, the PVCC regulator draws current from PBIAS pin. The PBIAS pin voltage must not exceed 28V.
5	PVCC	Output of the primary side PVCC regulator, Connect a capacitor to primary ground PGND.
6	FREQ	Switching frequency programming pin. Refer to the typical application schematic, one external resistor between VIN and FREQ and one capacitor connected between FREQ pin and PGND, are used to set the switching frequency. See Application Section for more details.
7	SS	Soft-start programming pin. A capacitor between the SS pin and PGND pin to set soft-start time.
8	EN	Enable input, with internal pull-up current source. Pull below 1.2V to disable. Float to enable. The pin can be used to set an adjustable undervoltage lockout with a resistive divider.
9	PGOOD	Power good indicator. This pin is an open-drain output. A 10kΩ pullup resistor between PGOOD and SVCC or an external logic supply pin is recommended.
10	COMP	Output of the error amplifier. An external RC compensation network connected between COMP and SGND compensates the converter control loop.
11	FB	Feedback pin for output voltage regulation. Connect a resistor divider network from the output of converter to the FB pin.
12	SGND	Secondary Side Ground.
13	SVCC	Output of the secondary side SVCC regulator, Connect a capacitor to secondary ground PGND.
14	SBIAS	Input to secondary side SVCC bias regulator.
15	CSN	Negative input to current sense amplifier, connect this pin to the VOUT side terminal of the capacitor of the RC network, refer to the typical application schematic.
16	CSP	Positive input to current sense amplifier, connect this pin to the SGND side terminal of the capacitor of RC network, refer to the typical application schematic.

Wide Body SOIC-16

Top View



16-Lead 10.3mm x 7.5mm x 2.65mm
SOIC Package

XX = Device Code, YY = Date Code, Z = Serial Number

Absolute Maximum Ratings[1]

(T_A = 25°C unless otherwise noted)

Symbol	Description	Value	Units
VIN, EN, FREQ	High Voltage Pins	-0.3 to 100	V
PBIAS	Medium Voltage Pins	-0.3 to 30	V
SW	High Voltage Pins (100µs duration,10%Duty)	-2 to 150	V
PVCC, SVCC, PGOOD	Low Voltage Pins	-0.3 to 6	V
SS, FB, COMP	Low Voltage Pins	-0.3 to 6	V
CSN, SBIAS	Medium Voltage Pins	-0.3 to 54	V
CSP	Low Voltage Pins	-0.3 to 6	V
T_J	Junction Temperature Range	-40 to 150	°C
T_s	Storage Temperature Range	-55 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

ESD Ratings[2]

Symbol	Description	Value	Units
V(ESD) Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins	±2000	V
	Charged device model (CDM), per JEDEC specification JESD22-C101, all pins	±500	

Thermal Capabilities[3]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	87.0	°C/W
Θ_{JC}	Thermal Resistance – Junction to Case	52.0	°C/W
P_D	Maximum Power Dissipation	1.4	W
$\Delta P_D/\Delta T$	Derating Factor above T_A = 25^{O}C	-11.5	mW/^{O}C

Ordering Information

Part Number	Marking[4]	Junction Operating Temperature	Package
KTB1100EYAA-TE	XXYYZ	-40°C to +125°C	SOIC-16

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. ESD Ratings conform to JEDEC industry standards. Some pins may actually have higher performance. Ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.
3. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
4. XX = Device Code, YY = Date Code, Z = Serial Number.

Electrical Characteristics[5]

Typical values correspond to T_A = 25°C. Minimum and Maximum specs are applied over the full operating junction temperature range of -40°C to 125°C, unless otherwise noted. V_{IN} = 24V, unless otherwise noted.

Symbol	Description	Conditions	Min	Typ.	Max	Units
Supply and Enable						
VIN	Input Voltage Range		7		100	V
VIN UVLO	VIN Rising			5.2		V
	VIN Falling			5.0		V
I_{IN}	Non-Switching Operating Current	FB = 2V, PBIAS = 0V		2.5	4	mA
I_{SHDN}	Shutdown Supply Current	EN = 0V		2	5	µA
PVCC	PVCC Regulator Output Voltage	PBIAS = 0V, PVCC open		4.7		V
		PBIAS = 8 to 28V, PVCC open		4.9		V
	PVCC Maximum Output Current		15	30		mA
PBIAS	PBIAS Operating Voltage Range		8		28	V
	PVCC Regulator Input Switchover Threshold	VIN = 24V		7.5	8	V
EN	EN Pin Voltage to Enable the Device	EN rising	1.16	1.24	1.32	V
	Hysteresis	EN falling		140		mV
SBIAS	SBIAS Operating Voltage Range		3		48	V
SVCC	SVCC Regulator Output Voltage	SBIAS = 3 to 48V, SVCC open		3		V
	SVCC Maximum Output Current		5	10		mA
Power FET						
$R_{DS(on)}$	POWER MOSFET ON Resistance			430	650	mΩ
I_{DSS}	Drain to Source Leakage Current	EN = 0V, V_{SW} = 120V			10	µA
t_{ON}	FET Minimum ON Pulse Duration			150		ns
t_{OFF}	FET Minimum OFF Pulse Duration			350		ns
t_r	Rise Time	VDS = 48V		20		ns
t_f	Fall Time	VDS = 48V		15		ns

5. KTB1100 is guaranteed to meet performance specifications over the –40°C to +85°C operating ambient temperature range by design, characterization and correlation with statistical process controls.

Electrical Characteristics[5] (continued)

Typical values correspond to T_A = 25°C. Minimum and Maximum specs are applied over the full operating junction temperature range of -40°C to 125°C, unless otherwise noted. V_{IN} = 24V, unless otherwise noted.

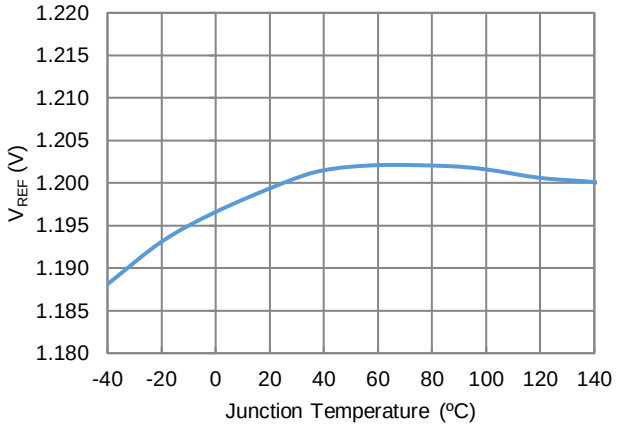
Symbol	Description	Conditions	Min	Typ.	Max	Units
Primary Side OCP						
I_{LIM}	Power MOSFET Current Limit Threshold		1.5	1.9	2.4	A
	Consecutive Cycles of Cycle-by-Cycle Current Limiting Events before Entering Hiccup Mode			32		
	Blanking Time in Hiccup Mode			256		ms
Secondary Side Current Sense						
I_{CSP}	CSP Pin Input Bias Current			50		nA
I_{CSN}	CSN Pin Input Bias Current			50		nA
G_{CS}	Current Sense Gain			10		V/V
FB and Error Amplifier						
V_{REF}	Feedback Voltage Reference		1.182	1.2	1.218	V
Gm	Error Amplifier Transconductance[6]		240	300	360	µS
R_{OUT}	Error Amplifier Output Resistance			10		MΩ
f_{BW}	Unity Gain Bandwidth			2		MHz
I_{FB}	Error Amplifier Input Bias Current			20		nA
I_{COMP}	COMP Sink Current	$V_{FB} = V_{REF}$ + 300 mV		200		µA
	COMP Source Current	$V_{FB} = V_{REF}$ - 300 mV		200		µA
OV UV and PGOOD						
PGOOD	PGOOD High Threshold (OV) with Respect to V_{REF}	V_{FB} Rising	107	110	115	%
	PGOOD High Hysteresis with Respect to V_{REF}			2		%
	PGOOD Low Threshold (UV) with Respect to V_{REF}	V_{FB} Falling	87	90	93	%
	PGOOD Low Hysteresis with Respect to V_{REF}			2		
Frequency and SS						
f_{SW}	Switching Frequency Range[6]		100		1000	kHz
I_{SS}	Soft-start Pull-up Current			5		µA
Thermal Shutdown						
T_{J_SHDN}	Thermal Shutdown Set Threshold	T_J rising		150		°C
T_{J_hys}	Thermal Shutdown Hysteresis			30		°C
Insulation Specifications						
V_{ISO}	Isolation Voltage	1 minute duration, ac RMS	3			kV

6. Guaranteed by design, characterization and statistical process control methods; not production tested.

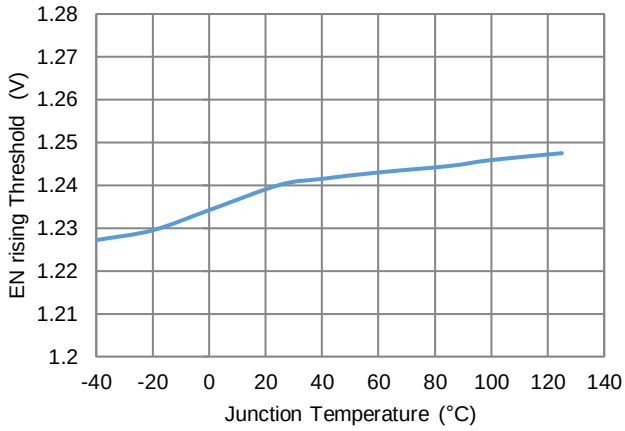
Typical Characteristics

V_{IN} = 9V-75V, V_{OUT} = 12V, R_{FREQ} = 121kΩ, C_{FREQ} = 680pF, Transformer (Np:Ns = 10:7, Lp = 35µH), T_J = 25°C unless otherwise specified.

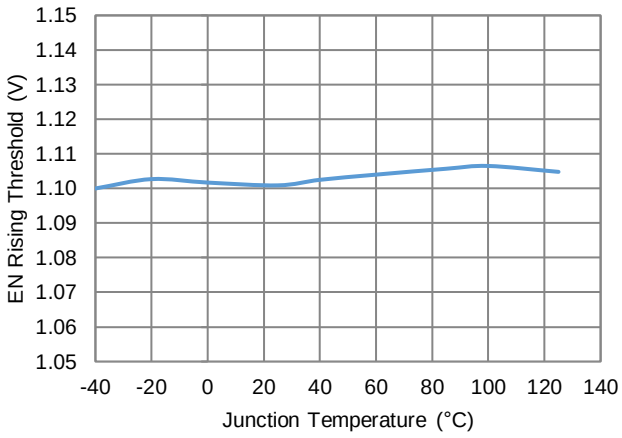
V_{REF} Temperature Regulation



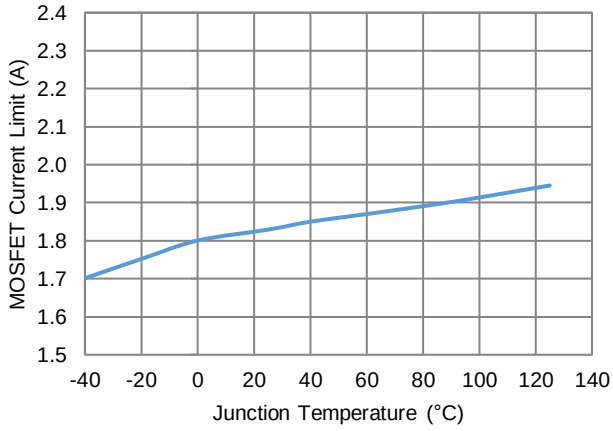
EN Rising Threshold vs Temperature



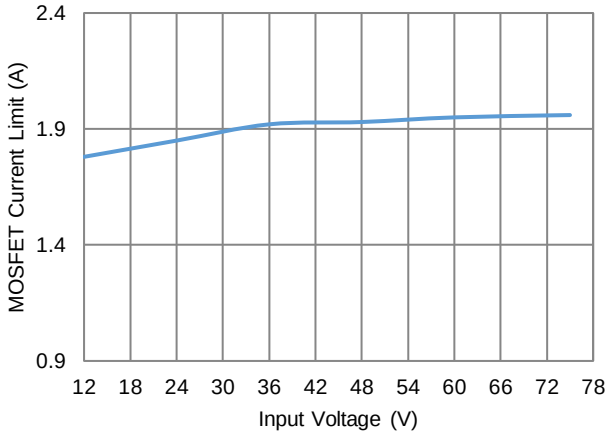
EN Falling Threshold vs Temperature



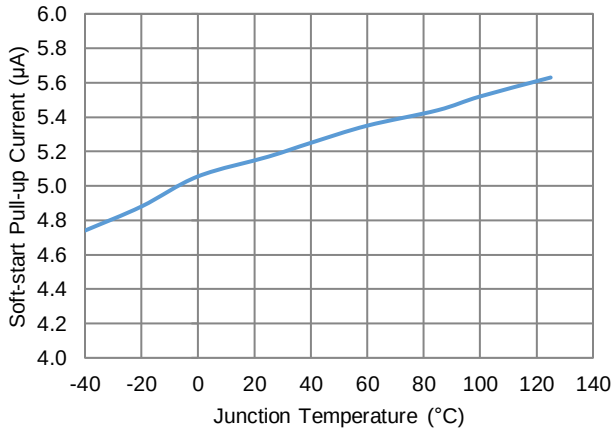
MOSFET Current Limit vs Temperature



MOSFET Current Limit vs Input Voltage



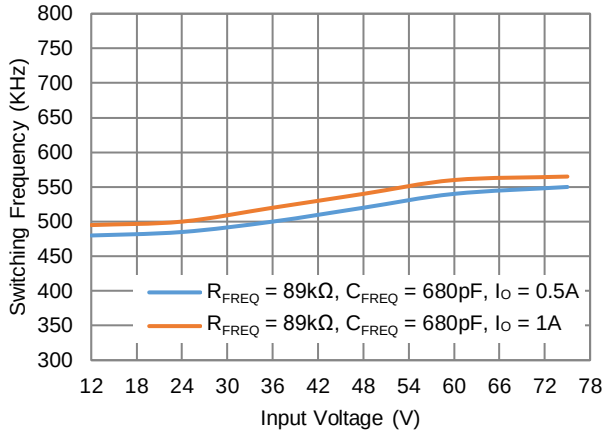
Soft-start Pull-up Current vs Temperature



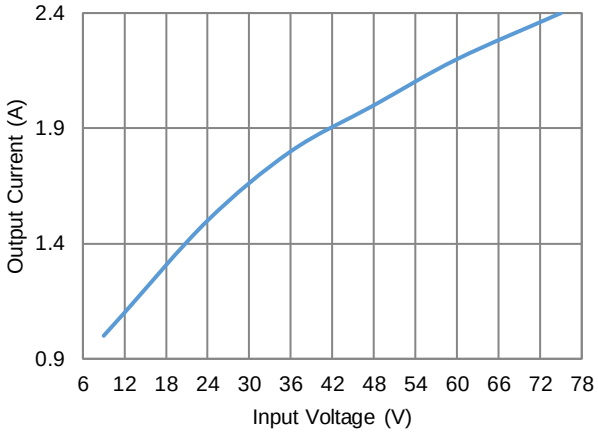
Typical Characteristics – 12V Output

V_{IN} = 9V-75V, V_{OUT} = 12V, R_{FREQ} = 121kΩ, C_{FREQ} = 680pF, Transformer (Np:Ns = 10:7, Lp = 35µH), T_J = 25°C unless otherwise specified.

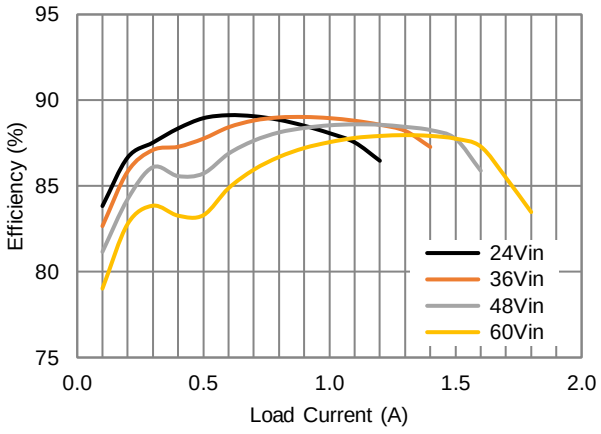
Switching Frequency vs Input Voltage



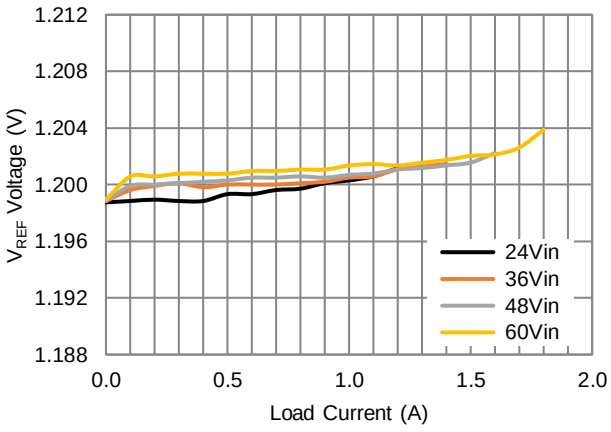
Maximum Output Current vs Input Voltage



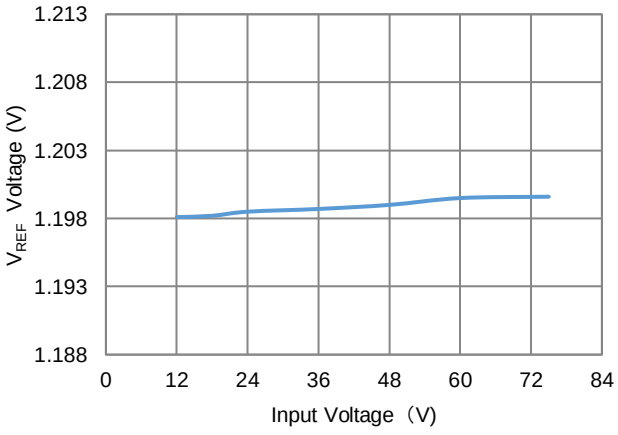
Efficiency



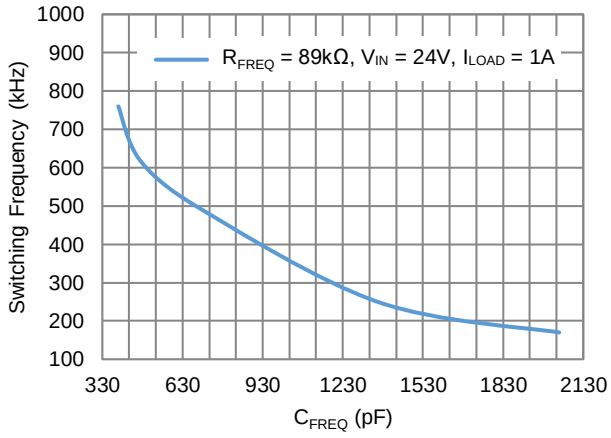
V_{REF} Load Regulation



V_{REF} Line Regulation



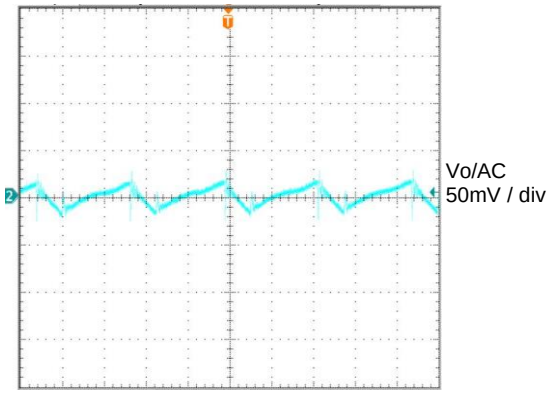
Switching Frequency vs Capacitance



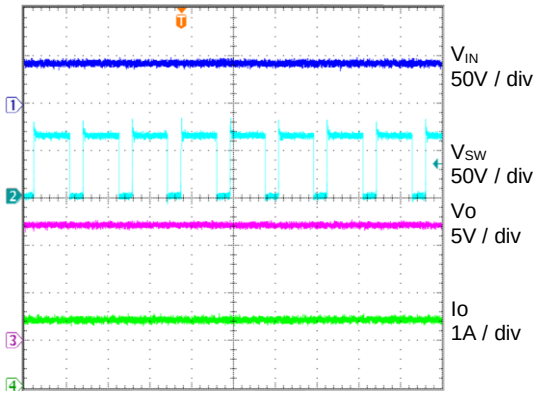
Typical Characteristics – 12V Output

V_{IN} = 9V-75V, V_{OUT} = 12V, R_{FREQ} = 121kΩ, C_{FREQ} = 680pF, Transformer (Np:Ns = 10:7, Lp = 35µH), T_J = 25°C unless otherwise specified.

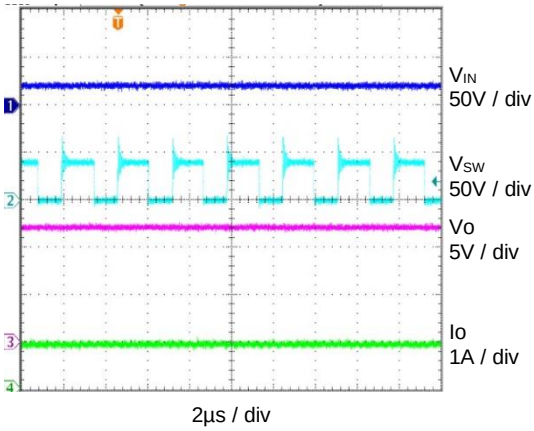
Output Ripple
(48V_{IN}, 12V_O, I_O = 2A, C_O = 150µF)



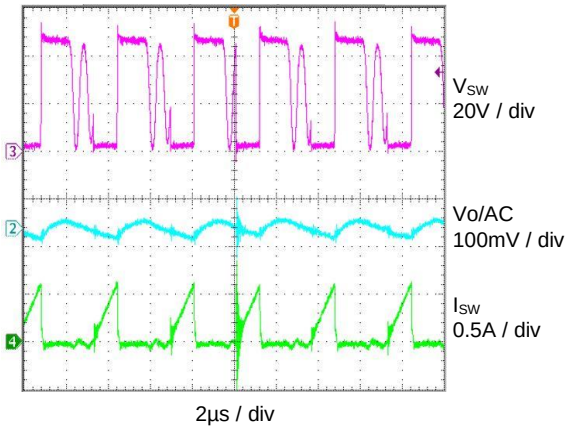
Stable Working at CCM
(48V_{IN}, 12V_O, I_O = 1.5A)



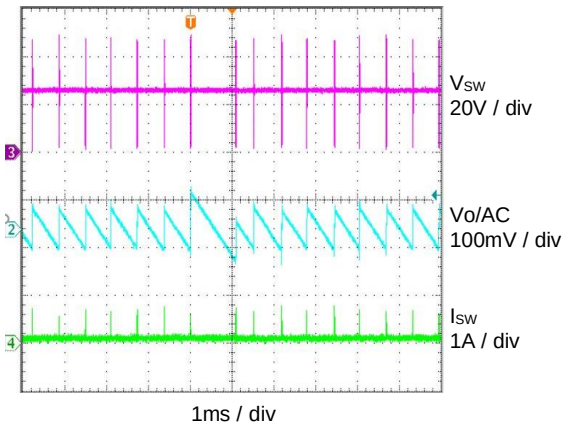
Stable Working at CCM
(24V_{IN}, 12V_O, I_O = 1A)



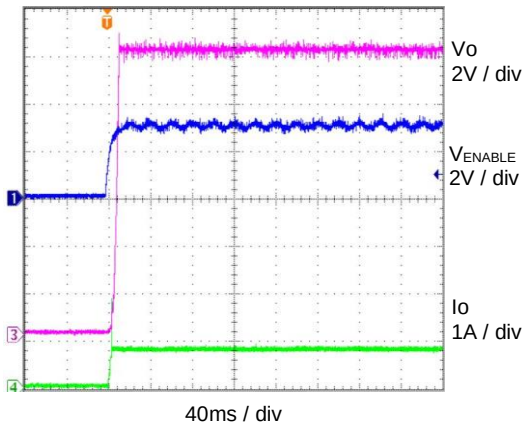
Stable Working at DCM
(24V_{IN}, 12V_O, I_O = 0.2A)



Stable Working at Burst Mode
(24V_{IN}, 12V_O, I_O = 0A)



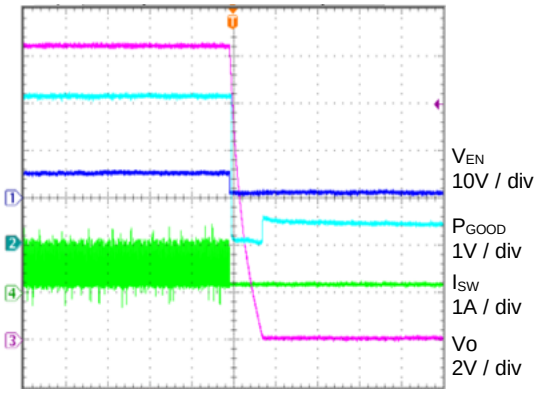
Enable Startup
(24V_{IN}, 12V_O, I_O = 1A)



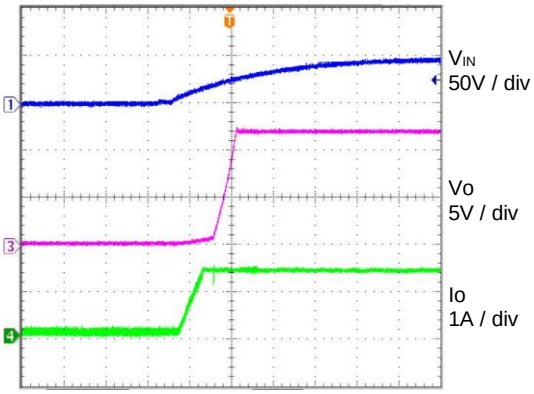
Typical Characteristics – 12V Output

V_{IN} = 9V-75V, V_{OUT} = 12V, R_{FREQ} = 121kΩ, C_{FREQ} = 680pF, Transformer (Np:Ns = 10:7, Lp = 35µH), T_J = 25°C unless otherwise specified.

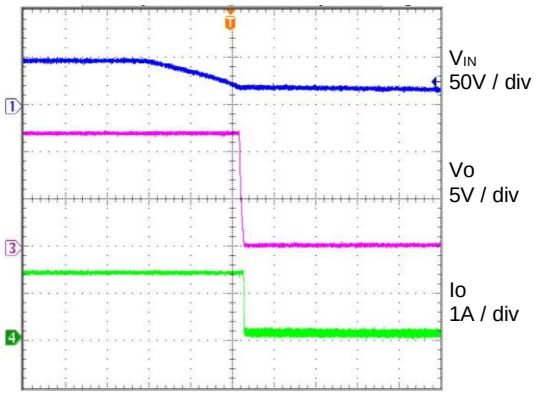
Enable Turn Off
($24V_{IN}$, $12V_O$, I_O = 1A)



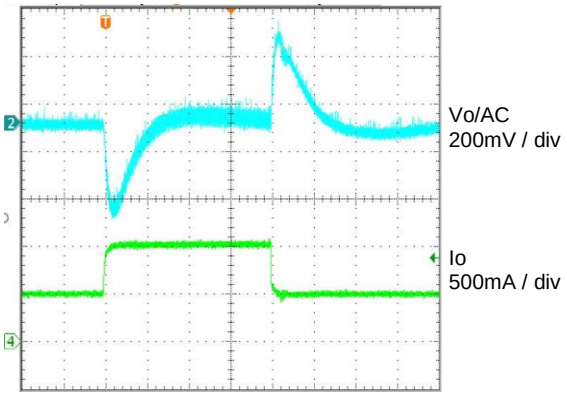
Input Startup
($48V_{IN}$, $12V_O$, I_O = 1.5A)



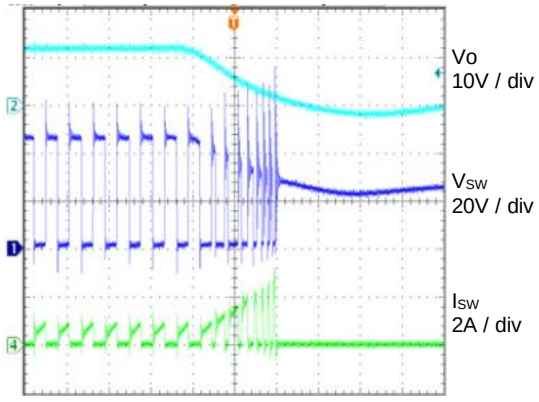
Input Shutdown
($48V_{IN}$, $12V_O$, I_O = 1.5A)



Dynamic Load Performance
($24V_{IN}$, $12V_O$, Load Step from 0.5A-1A-0.5A)



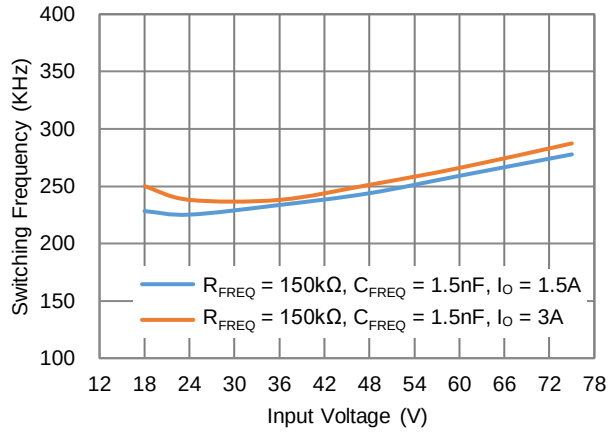
Short Circuit Performance
($12V_O$, I_O from 1A to Short)



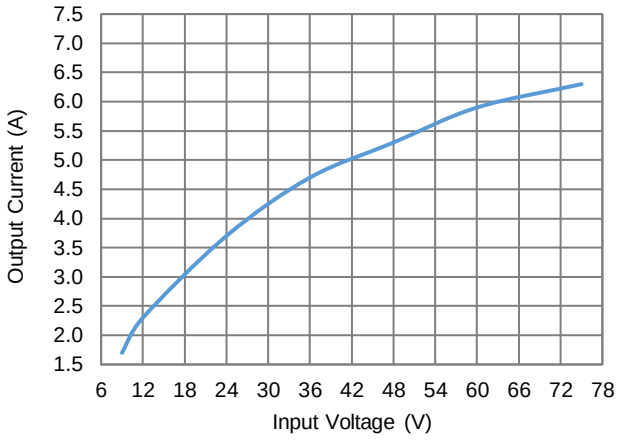
Typical Characteristics – 5V Output

V_{IN} = 9V-75V, V_{OUT} = 5V, R_{FREQ} = 150kΩ, C_{FREQ} = 1.5nF, Transformer (Np:Ns = 6:1, Lp = 120µH), T_J = 25°C unless otherwise specified.

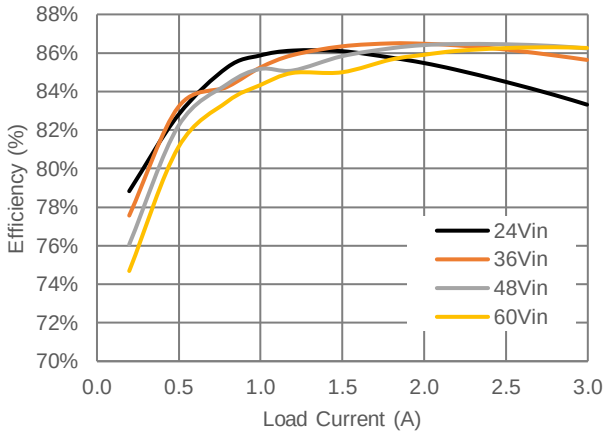
Switching Frequency vs Input Voltage



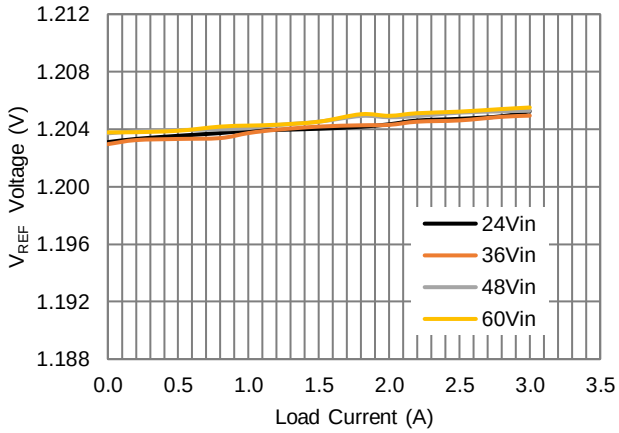
Maximum Output Current vs Input Voltage



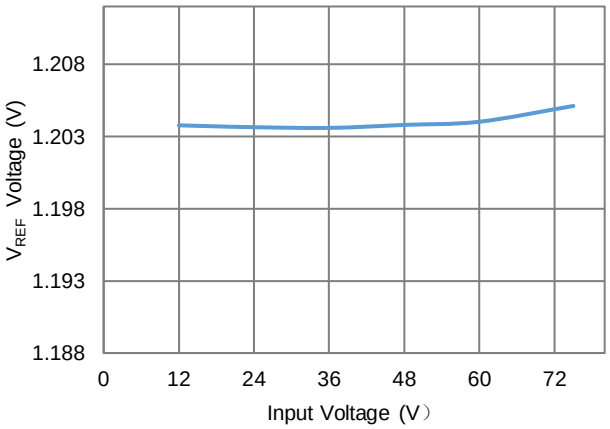
Efficiency



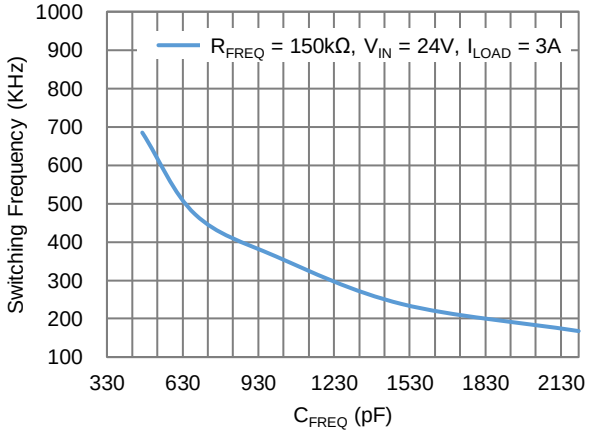
V_{REF} Load Regulation



V_{REF} Line Regulation



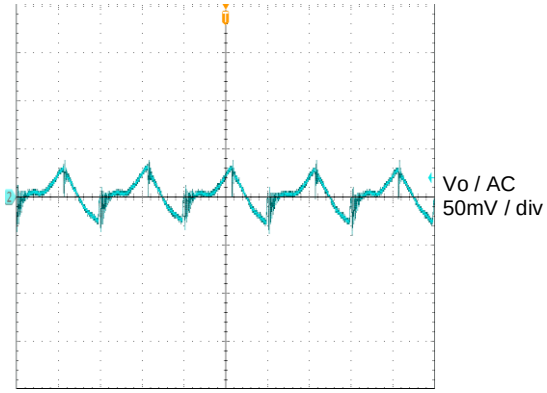
Switching Frequency vs Capacitance



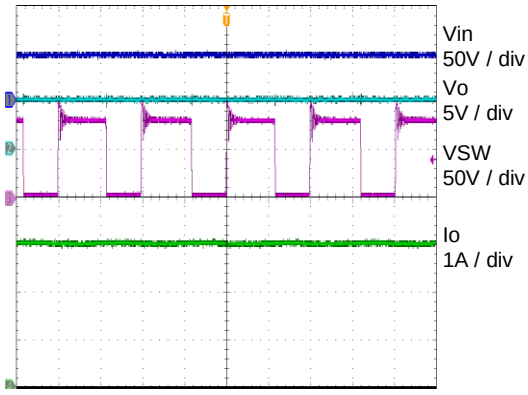
Typical Characteristics – 5V Output

V_{IN} = 9V-75V, V_{OUT} = 5V, R_{FREQ} = 150kΩ, C_{FREQ} = 1.5nF, Transformer (Np:Ns = 6:1, Lp = 120µH), T_J = 25°C unless otherwise specified.

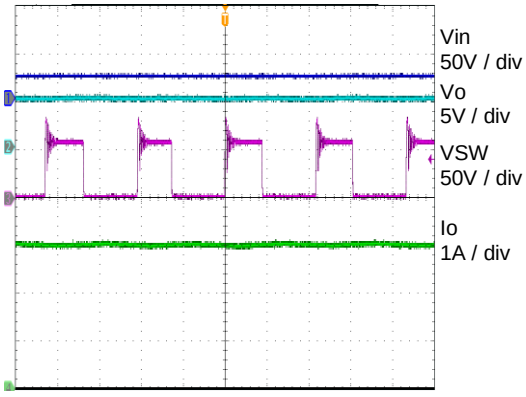
Output Ripple
(48V_{IN}, 5V_O, I_O = 3A, C_O = 47µF)



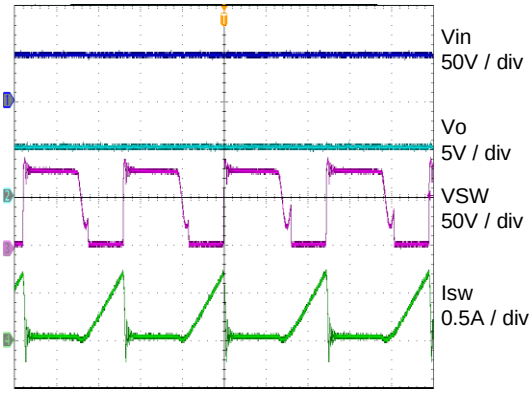
Stable Working at CCM
(48V_{IN}, 5V_O, I_O = 3A)



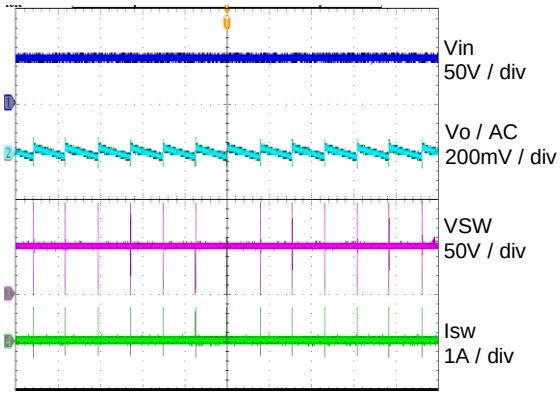
Stable Working at CCM
(24V_{IN}, 5V_O, I_O = 3A)



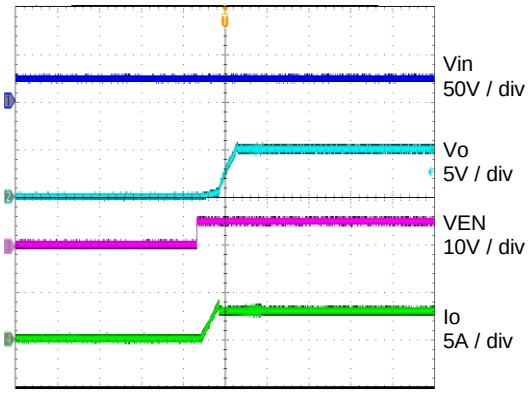
Stable Working at DCM
(24V_{IN}, 5V_0, I_0 = 1A)



Stable Working at Burst Mode
(48V_{IN}, 5V_O, I_O = 0A)



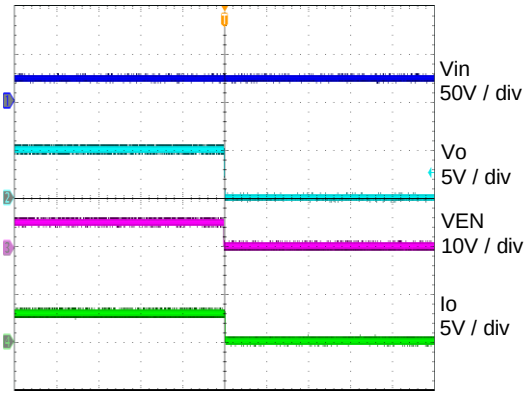
Enable Startup
(24V_{IN}, 5V_O, I_O = 3A)



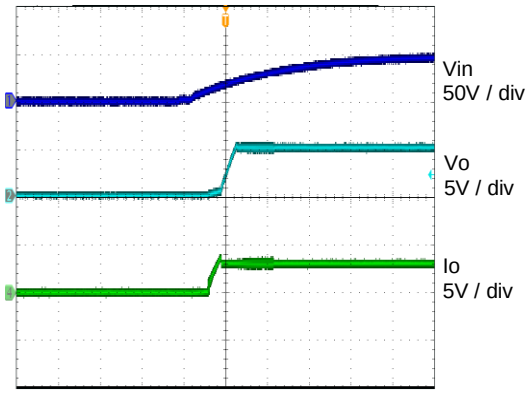
Typical Characteristics – 5V Output

V_{IN} = 9V-75V, V_{OUT} = 5V, R_{FREQ} = 150kΩ, C_{FREQ} = 1.5nF, Transformer (Np:Ns = 6:1, Lp = 120µH), T_J = 25°C unless otherwise specified.

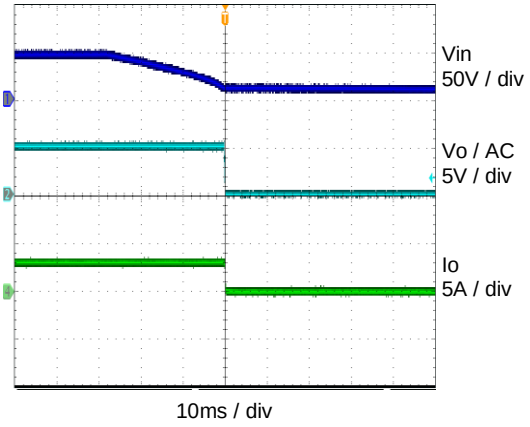
Enable Turn Off
(24V_{IN}, 5V_O, I_O = 3A)



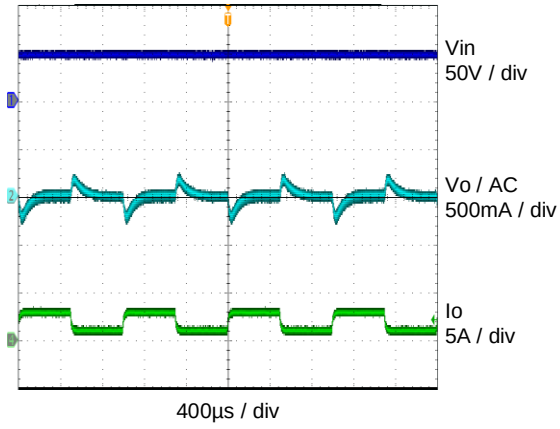
Input Startup
(48V_{IN}, 5V_O, I_O = 3A)



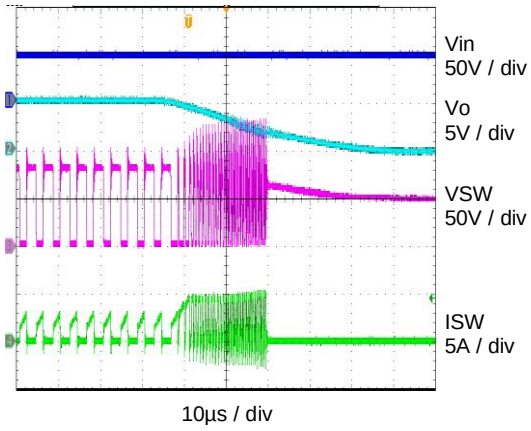
Input Shutdown
(48V_{IN}, 5V_O, I_O = 3A)



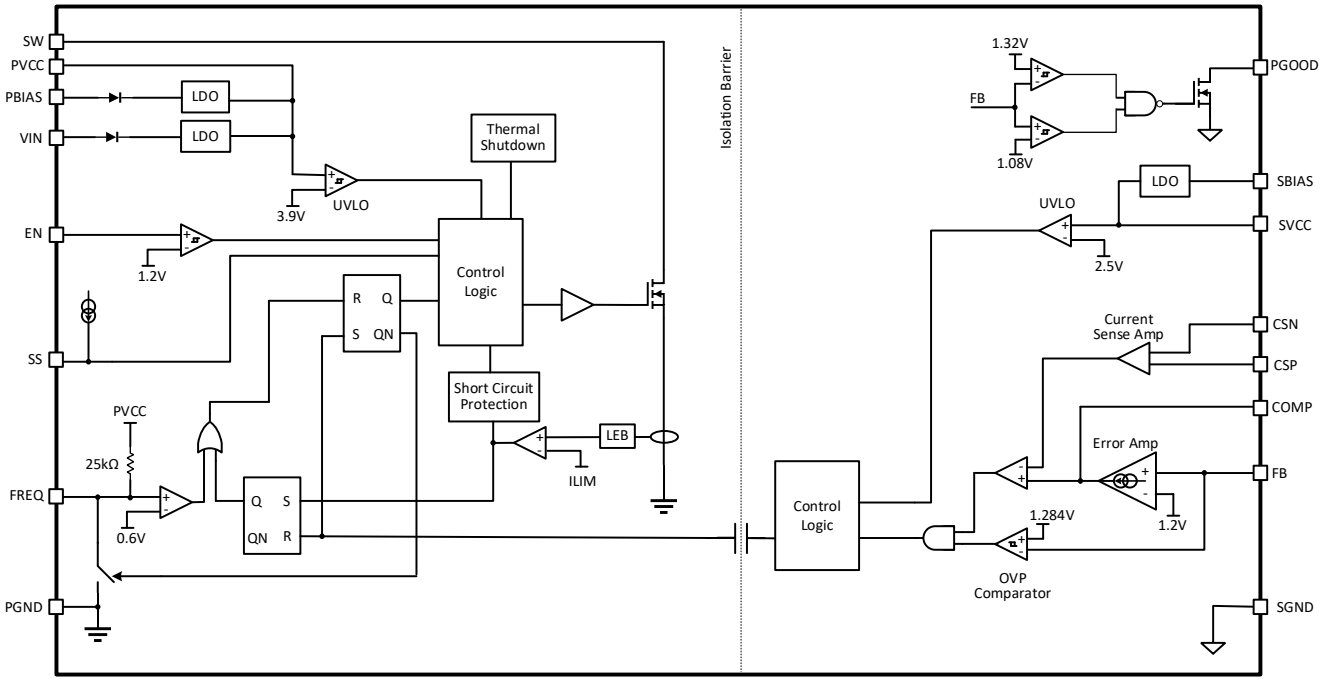
Dynamic Load Performance
(48V_{IN}, 5V_O, Load Step from 1A-3A-1A)



Short Circuit Performance
(48V_O, 5Vo, I_O from 3A to Short)



Block Diagram



Functional Description

Overview

The KTB1100 is a highly integrated isolated flyback regulator with digital isolator, integrated primary power MOSFET and secondary feedback circuit. It employs current-mode constant on-time (COT) control. KTB1100 offers a complete solution for an isolated flyback dc-to-dc power supply by integrating the 3kV digital isolator, the primary MOSFET and secondary feedback circuitry in one package. The device operates over a wide input voltage range from 7V to 100V supporting a variety of applications. The output voltage can be set by an external resistive divider, allowing KTB1100 to be used in many applications.

Digital isolator is integrated in the KTB1100 to eliminate the optocoupler that transmit the output voltage condition from secondary to primary. Integrating the digital isolator reduces system design complexity, cost, and component count and improves overall system performance and reliability. Traditionally in a flyback converter, a discrete optocoupler is used in the feedback path to transmit the signal from the secondary to the primary side. However, the current transfer ratio (CTR) of optocouplers can degrade over time and over temperature. If it is not considered during the design, it can reduce the long-time system reliability. Secondly, most discrete optocouplers used in telecom or industrial applications have a maximum operation temperature of approximately 100°C to 125°C, potentially limiting the maximum operating temperature of the system.

The KTB1100 eliminates the use of a discrete optocoupler, thereby reducing system cost, PCB area, and complexity, while improving system reliability and increasing the maximum operating temperature of the system.

The primary-side 150V power MOSFET is integrated in the KTB1100 to reduce system cost and size. This primary 150V power MOSFET has a 0.43Ω RDS_ON and can work up to a peak current of 1.9A before current limit is triggered. The KTB1100 primary-side MOSFET incudes a current limit function and when the current

exceeds its peak current limit for 32 cycles, the KTB1100 will shut down and enters hiccup mode with a 256ms time interval.

Secondary feedback circuitry is integrated in the KTB1100 to eliminate external voltage reference and error amplifier. The integrated voltage reference has a better than ±1% accuracy, while the error amplifier has a high gain bandwidth.

The primary circuitry in the KTB1100 includes a 4.8V LDO, a primary power MOSFET with current sensing, optional bias circuit, and PWM generator. The secondary circuitry includes the error amplifier, an internal voltage reference, a 3V LDO regulator, and a dedicated pin for power good indication.

PWM signal is controlled both by the constant on-time control of the primary side and the valley current mode control in the secondary side of KTB1100. Current sensing is performed on the secondary side by sensing the output current of the secondary transformer winding cycle by cycle. The output voltage of the converter is sensed by the error amplifier on the secondary side, sending a signal to the primary side via the 3kV integrated digital isolator for a complete control loop solution.

KTB1100 offer features such as input undervoltage lockout (UVLO), precision enable with hysteresis, output overload current limit (OCL) short circuit protection (SCP), output overvoltage protection (OVP), over temperature protection (OTP), and power saving with burst mode in light load conditions.

Enable

KTB1100 flyback regulator is turned on and off using the EN pin. If the EN pin is high or floating the regulator is enabled. Pulling the EN pin low will disable the regulator. EN pin maximum rating voltage allows connection to Vin pin for simple control. Enable high logic threshold is 1.24V with a 0.1V hysteresis voltage.

Connecting a resistive divider between EN and VIN sets the input start-up voltage with hysteresis.

To prevent noise, it is recommended to connect a capacitor on the EN pin to PGND. Please refer to the application circuit in Figure 1.

Soft-Start

To provide a controlled startup, a capacitor is required on the SS pin. At device power on, the SS capacitor is slowly charged by an internal 5µA current source, increasing the switching frequency thereby limiting the input in-rush current. This will slowly increase until the operating switching frequency set by R_{FEQ} and C_{FEQ} is reached.

Internal Switching FET

The SW and PGND provide connection to the drain and source of the integrated switching power MOSFET. This 150V MOSFET has a typical 0.43Ω RDS_ON. It is used as a primary power switch for the flyback DCDC converter. The internal MOSFET gate driver is powered from PVCC voltage rail, and the return path is through the GND pin. As the large leakage inductance of the flyback transformer and high peak current of primary power MOSFET, there will be a high voltage stress produced on the SW node of KTB1100, especially at high input voltage. Therefore, a RCD snubber circuit for SW node is recommended. It is recommended that RCD values are selected to keep the voltage at SW at less than 120V during normal operation.

Primary Optional Bias Supply

There is an optional input to primary side PVCC bias regulator that can be powered from an external supply instead of VIN. This can reduce the power loss at high input voltages. For PBIAS > 8V, the PVCC regulator draws current from PBIAS pin. The PBIAS pin voltage must not exceed 28V. For most applications, it is recommended to use PBIAS function for higher system efficiency when input voltage is over 48V. An auxiliary primary winding of the transformer is generally used for this function.

Primary Side PVCC Regulator

A high voltage LDO regulator is connected to the VIN or PBIAS and provides a regulated output at PVCC. PVCC is the output of the primary side PVCC regulator, to power the internal FET gate driver and other internal control circuitry. Connect a 1µF capacitor from PVCC to primary ground PGND. PVCC is 4.7V when regulated from VIN. If a voltage over 8V is supplied through PBIAS, the PVCC pin voltage is 4.9V.

Secondary Bias Supply

SBIAS is the input to secondary side SVCC bias regulator. SBIAS is a high voltage input that can be directly connected to the output voltage. Alternatively, it can be also connected to an auxiliary secondary winding of transformer to improve system efficiency.

Secondary Side SVCC Regulator

SVCC is the output of the secondary side SVCC regulator and is typically 3V. Connect a 1µF capacitor to secondary ground PGND.

Frequency

Switching frequency can be programmed by an external resistor, Rfeq, connected between VIN and FREQ and an external capacitor, Cfeq, connected from FREQ to PGND, as shown in figure 1.

The switching frequency during CCM (continuous current mode), is constant and reduces during DCM (discontinuous current mode). During light load, the regulator will enter burst mode, only switching to replenish the output capacitor to save power and therefore increase the system efficiency.

Compensation

An external RC compensation network connected between COMP (output of the error amplifier) and SGND compensates the converter control loop to provide system stability.

Current Sense

An external RC network is required for the current sense signal function. The current sense signal should be differentially sensed by CSP and CSN. For further details please refer to the application circuit in figure 1 and the layout guidelines.

Power Good

KTB1100 has a power good indicator. This pin is an open-drain output. A 10kΩ to 100kΩ pullup resistor between PGOOD and SVCC or an external logic supply.

Thermal Protection

The KTB1100 provides thermal protection by the continuous monitoring of the die junction temperature. Thermal protection is triggered when the die junction temperature reaches 150°C. When the die junction temperature falls below 120°C, the KTB1100 will be turned on again.

Application Information

Typical Application Circuit

Figure1 is the application circuit of KTB1100. The KTB1100 is a highly integrated isolated flyback regulator with digital isolator, primary power MOSFET and secondary feedback circuit. It can offer a complete solution for an isolated flyback dc-to-dc power supply. The flyback power supply is typically used to convert a wide input range DC voltage to an isolated DC output voltage. The device can operate over a wide input voltage range from 7V to 100V to support a variety of applications. The output voltage can be programmed to a variety of voltages such as 5V, 12V, 24V and 48V. This section presents a simplified discussion of the design process.

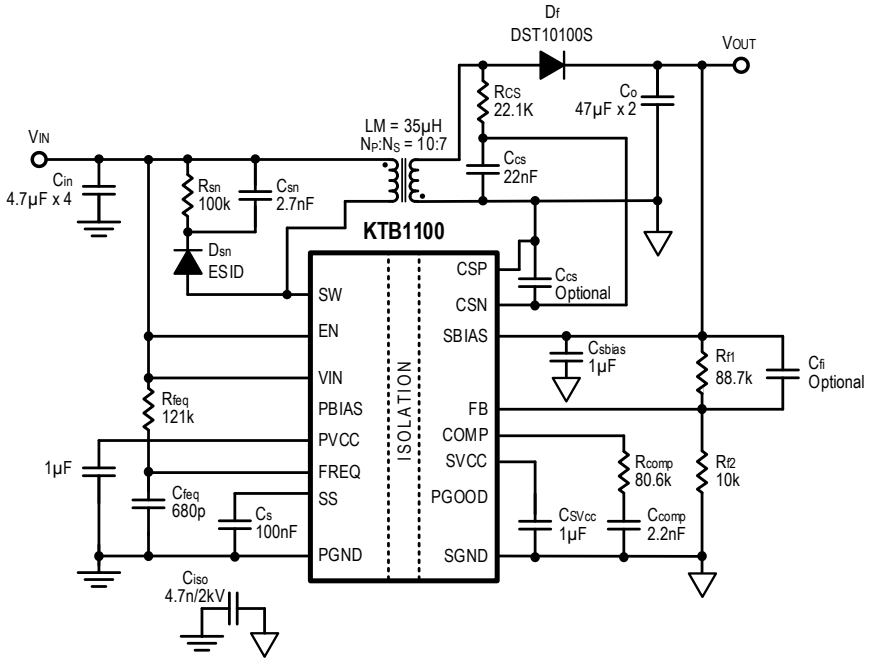


Figure 1. Application Circuit

Transformer **Design**

The transformer design should consider the input voltage, output voltage and transformer size. The key electrical parameters of the transformer are turns ratio, inductance, saturation current and so on.

For the transform design, we usually design turn ratio first, then we design the inductance of transform, finally we design the saturation current of transform. Below is reference design procedure for a transformer design, the transform parameters need a comprehensive consideration through turn ratio, inductance and saturation current, power MOSFET and diode voltage stress and so on.

The transformer turns ratio is calculated as follows:

$$n = \frac{Vin\_min * Dmax}{(Vo_{max} + Vd) * (1 - Dmax)}$$ Equation (1)

Where,

n = the turns ratio from primary winding to secondary winding

Vin_min = the min. operating input voltage

Vo_max = the max. output voltage

Vd = the forward voltage drop of secondary rectifier diode.

Dmax = max. duty cycle, (the max. duty cycle of the flyback converter is approx. 70%)

The flyback transformer primary inductance is calculated as follows:

$$Lm = \frac{n * Vin * D * (1 - D)}{Fsw * Io * Kc}$$ Equation (2)

Where,

Lm = the primary inductance of flyback transformer

n = the turns ratio from primary winding to secondary winding

Vin = the operating input voltage

D = duty cycle.

Fsw = Switching frequency

Io = Output current

Kc = is the ripple current coefficient compared with output current. The value of Kc is normally selected between 0.5 to 1.5

The primary side peak current is calculated as follows:

$$Ipeak = \frac{Io}{n * (1 - D)} + \frac{Vin * D}{2Fsw * Lm}$$ Equation (3)

Where,

Io = Output current

n = the turn ratio from primary winding to secondary winding

D = duty cycle

Vin = the operating input voltage

D = duty cycle

Fsw = Switching frequency

Lm = the primary inductance of flyback transformer

Frequency Setting

The KTB1100 employs current-mode, constant on-time (COT) control for fast transient response as well as superior output voltage regulation. The switching frequency of KTB1100 can be set by the value of Rfeq and Cfeq as shown in figure 1. To set the frequency, first choose the value of Rfeq, and then set the Cfeq to achieve the target switching frequency, as shown in the following:

$$Rfeq = \frac{n*Vo*Ri}{Vdd}$$ Equation (4)

$$Fsw = \frac{n*Vo}{Vt*Rfeq*Creq}$$ Equation (5)

Where,

n = the turn ratio from primary winding to secondary winding

Vo = the target output voltage

Ri = the internal resistance of KTB1100, internally fixed at 25kΩ

Vdd = the internal power supply of KTB1100, internally fixed at 4.8V

Vt = the internal comparator threshold of KTB1100, internally fixed at 0.6V

Rfeq = the frequency set resistor

Cfrq = the frequency set capacitor

Current Sense RC Net Setting

The KTB1100 uses the secondary current sense signal for control. The correct Rcs and Ccs values are calculated as follows:

$$Rcs * Ccs = K * \frac{Lo}{DCR}$$ Equations (6)

Where,

Lo = the inductance of the secondary side transformer winding,

DCR = the resistance of the secondary side transformer winding.

Rcs = the resistor of current sense RC network. Its value should be as large as possible to minimize the power dissipation. A recommend value is between10kΩ and 100kΩ.

Ccs = the capacitor of current sense RC network.

K = the coefficient, with a typical value of 1, and the suggested range is between 0.5 and 1.5.

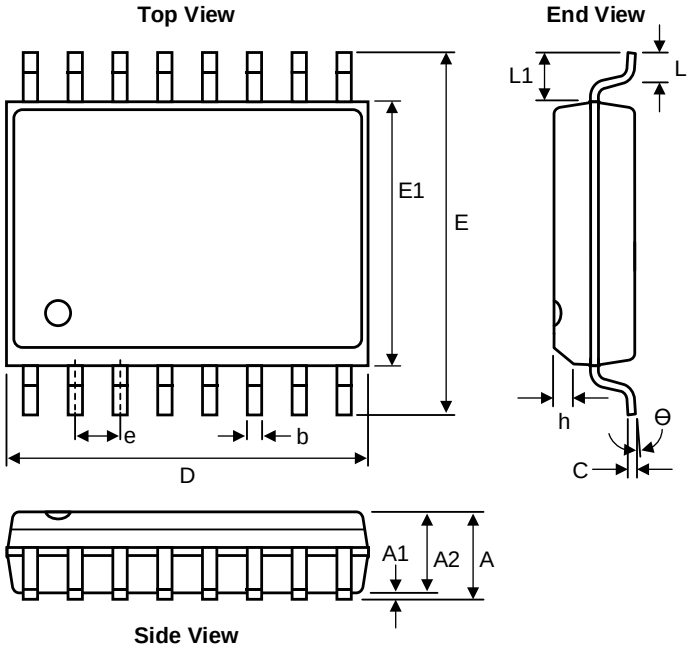
PCB Layout Guidelines

The following guidelines are recommended for optimum performance.

1. Keep the power stage loop area as small as possible. This includes the input loop (Cin, Transformer, Internal FET of KTB1100) and the output loop (Transformer, Co, Rectifier Diode).
2. Use a single point connection between signal GND (SGND of KTB1100) and output power GND (The negative terminal of the output voltage).
3. Ground all the control capacitors to their respective grounds and place the control circuit capacitors close to the IC to decouple noise.
4. Keep the primary and secondary control circuit trace far away from noise sources (such as primary switch node and secondary switch node).
5. CSP and CSN pins should differentially sense the current signal through the sense components. A 100Ω to 1kΩ filter resistor is suggested in series with each CSP and CSN pins. The CSP and CSN traces should not cross any switch nodes.
6. Keep FB and COMP pins far from high noise sources. In some high output current applications, a typically 10kΩ resistor is suggested to insert between FB pin and output resistor divider network to filter noise.
7. As snubber circuit like RCD should be used to limit peak voltage on the SW pin at turn-off. Minimize the loop from the RCD snubber components to the transformer and IC.

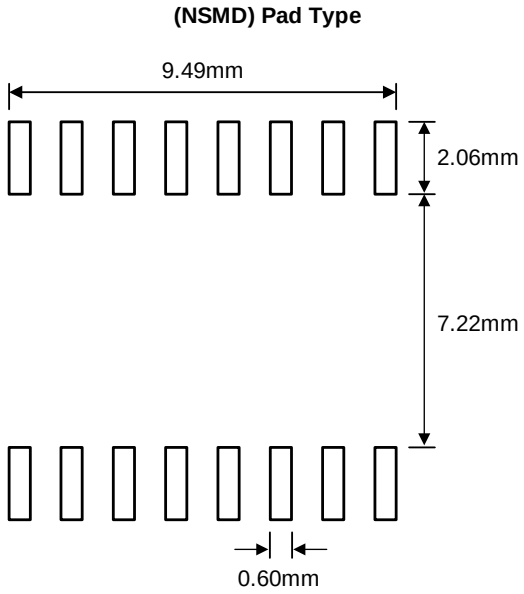
Packaging Information

SOIC-16 (10.30mm x 7.50mm x 2.65mm)



Dimension	mm		
	Min.	Typ.	Max.
A	2.15	–	2.65
A1	0.10	–	0.30
A2	2.05	–	2.55
b	0.31	–	0.51
C	0.10	–	0.33
D	10.10	10.30	10.50
E	9.97	10.30	10.63
E1	7.40	7.50	7.60
e	1.27 BSC		
h	0.25	–	0.75
L	0.40	–	1.27
L1	1.4 BSC		
Θ°	0	–	8

Recommended Footprint



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