IEEE 802.3bt-Compliant, PoE Powered Device with DC-DC Controller

Features

- IEEE® Std. 802.3af/at/bt compliant operation
- Input power levels up to 90W
- PoE PD Class 0-8 power capability (up to 72W)
- Robust Type 1, 2, 3 and 4 PSE detector with proprietary line noise digital filtering
- Maintain Power Signature (MPS) for Type 1-4 PSE BT operation
- Supports up to 5 event classification
- Integrated PWM peak current mode controller
- 9.5V to 57V local power input supply range
- Supports high efficiency regulator topologies:
  - Flyback or Forward
  - Flyback or Forward with synchronous rectification
  - Flyback or Forward with active clamp
- Power conversion efficiency up to 92.6%
- Dual gate driver with dead time adjustment
- Internal slope compensation
- Programmable DC current limit up to 2.2A for 90W applications
- Low R_{DSON} 100V hot-swap FET (typical 0.13Ω)
- IEC 61000-4-2/3/4/5/6 EMC Compliant
- Programmable frequency dithering feature for spread-spectrum operation to reduce EMI
- Integrated Short-Circuit Protection (SCP) and Over Current Protection (OCP)
- Over Temperature Protection (OTP)
- Supports low power standby modes
- Auto class support
- 4x4mm, 32-lead WQFN package
- -40°C to +125°C Junction Temperature Range

Brief Description

The KTA1142 is a highly integrated CMOS IC containing PD controller and PWM regulator to form a single chip solution for IEEE® 802.3af/at and bt PoE applications.

This device provides all physical layer Powered Device (PD) functionality required by the IEEE® 802.3af-2003, IEEE® 802.3at-2009, IEEE® 802.3bt-2019 standards. This includes Class 8 (5 event) classification, Type 1-2 or 3-4 PSE detect indication, PD detection, under-voltage lockout (UVLO), and Hot-Swap FET integration.

The integrated DC/DC controller features adjustable slope compensation, load based DCM to CCM operation to maximize power conversion efficiency with dual complementary low-side drivers, programmable dead time, soft-start and soft-stop timing. The design architecture with optional frequency dithering will aid with improving radiated and conducted EMI performance. Additionally, the device provides safe, low-impedance ground discharge paths for superior reliability and circuit protection.

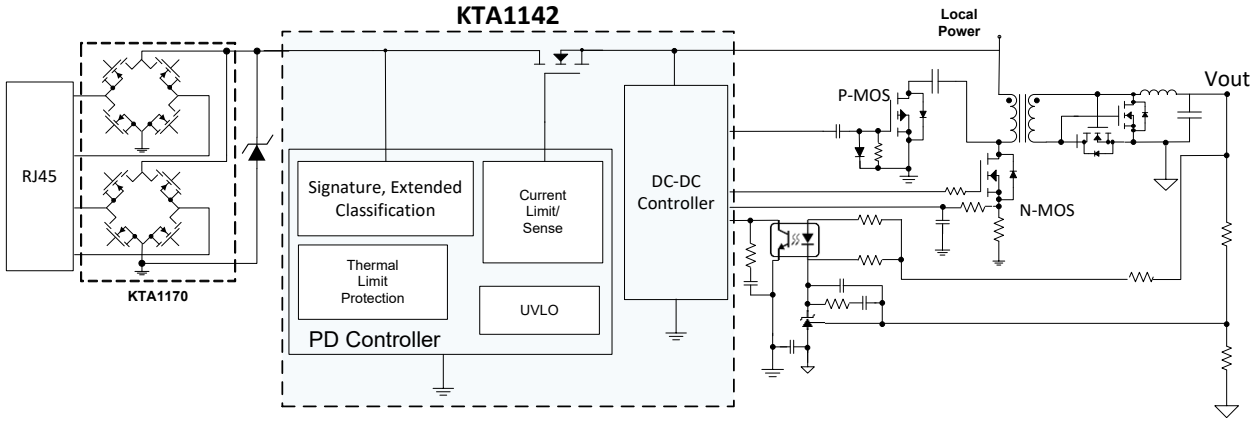
The controller is compatible with high efficiency Flyback or Forward topologies for system load levels up to 72 Watts. This makes the KTA1142 an ideal solution for Voice over IP (VoIP) Phones, and 5G/LTE Base Stations, Wireless LAN Access Point, Security Camera, and Notebook Computer applications.

The KTA1142 utilizes a space saving 4x4mm, 32-pin WQFN package to aid in compact printed circuit board designs while maximizing thermal performance. The device supports operation over a -40°C to 85°C ambient temperature range.

Applications

- Voice over IP (VoIP) phones
- Security and web cameras
- Lighting and High-Power Wireless Data Systems
- Wireless LAN access points, WiMAX terminals
- Point-of-Sale (POS) terminals, RFID terminals
- Thin clients and notebook computers
- Fiber-to-the-home (FTTH) terminals

Typical Application

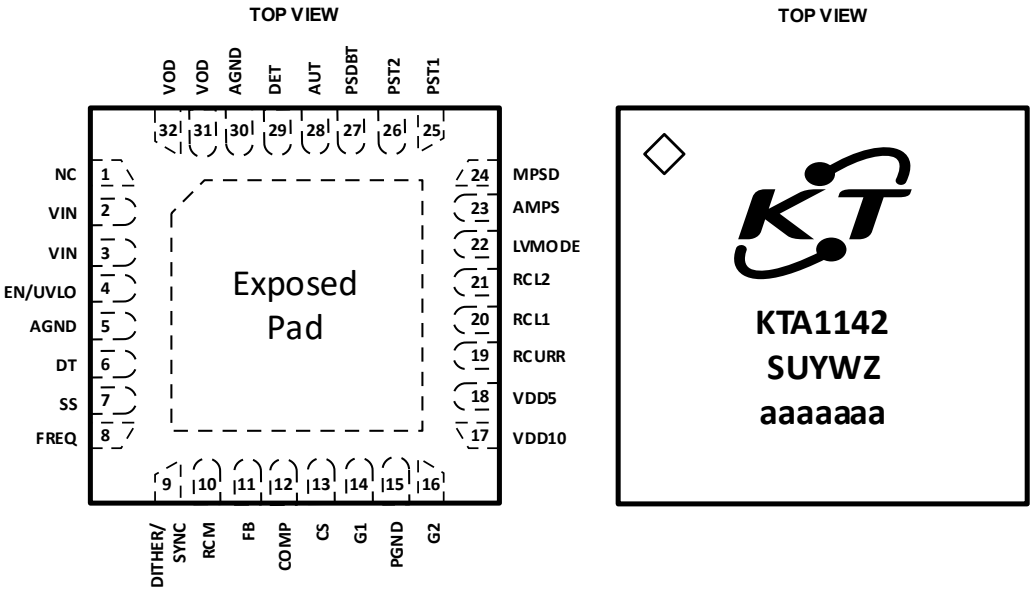


Ordering Information

Part Number	Marking[1]	Package
KTA1142EUAT-TB	SUYWZ aaaaaaa	WQFN44-32

Pinout Diagram

WQFN44-32



32-Lead 4mm x 4mm x 0.75mm
WQFN Package, 0.4mm pitch

Top Mark

SU = Device ID, YW = Date Code, Z = Serial Number
aaaaaaa = Assembly Lot Tracking Number

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Pin Descriptions

Pin #	I/O	Name	Function
1	-	NC	Not Connected.
2, 3	P	VIN	Positive bus pin that is fed by the output of the external diode bridge. This bus requires the connection of a detection signature capacitor and resistor. Refer to the Detection Mode section.
4	A/I	EN/UVLO	Enable, and Undervoltage detection and protection pin.
5	A	AGND	Analog ground pin.
6	A/I	DT	PWM gate control signal dead time setting pin. Connect a resistor between the DT pin and AGND to set gate control dead time. Refer to the Functional Description section dead time set discussion and equation to determine the desired resistor value.
7	A/I	SS	Soft-start/Soft-stop set pin. A capacitor connected from the SS pin to AGND sets the converter soft-start/soft-stop timing. A ceramic capacitor is recommended for accurate circuit operation over varied conditions.
8	A/I	FREQ	Switching frequency set. Connect a resistor connected from FREQ to AGND to set the internal oscillator frequency. Refer to the Functional Description section Frequency discussion and equation to determine the required resistor value.
9	A/I	DITHER/SYNC	Frequency Dithering Programming /Synchronization control pin. FREQ DITHER: For spread-spectrum frequency operation to improve system EMI performance, connect a capacitor from DITHER to AGND and a resistor from DITHER to FREQ pins. Refer to Equations 6 and 7 in the Functional Description section to determine capacitor and resistor values. SYNC: An external signal applied to this pin will synchronize the internal oscillator to a system source. Refer to the device electrical characteristics and applications section for sync signal limits and details.
10	A/I	RCM	Slope compensation programming input and resistor. A resistor connected from the RCM pin to AGND set the PWM control internal slope compensation. Refer to PWM comparator and slope compensation applications information determine the required value for the RCM resistor.
11	A/I	FB	Voltage mode feedback pin of internal error amplifier. For isolated regulator systems (optocoupler feedback), leave this pin connected to GND or +5V (VDD5). For non-isolated regulator systems, connect FB pin to the resistor divider sense network to regulate the output voltage
12	A/I	COMP	Connect the compensation network between the COMP and AGND. Non-isolated application circuits may be directly connected to this pin. Isolated systems should connect the compensation network via an optocoupler to the COMP pin.
13	A/I	CS	Current Sense feedback pin to sense peak current utilized for current mode control and for current limiting and protection of the application circuit.
14	O	G1	Primary gate driver output for the PWM control MOSFET.
15	P	PGND	Power Ground Pin.
16	O	G2	Secondary MOSFET gate driver output. The auxiliary gate driver output may be used for active clamp or synchronous rectification designs.
17	O	VDD10	Internal 10V regulator output pin. Bypass this output with a 1µF or greater value ceramic capacitor connected between VDD10 and AGND.
18	O	VDD5	Internal 5V regulator output pin. Bypass this output with a 1µF or greater value ceramic capacitor connected between VDD5 and AGND.
19	A/I	RCURR	Current limit set pin. This pin should be terminated to AGND through a resistor, directly connected to AGND or left open for the following modes: RCURR = short to AGND for AF operation, 5kΩ for AT operation, 10kΩ for BT1 operation, or leave Open for BT2 operation.
20	A/I	RCL1	Class type setting resister 1. Connect a resistor from RCL1 to AGND. Refer to Table 3 in the Functional Description section for RCL1 values.
21	A/I	RCL2	Class type setting resistor 2. Connect a resistor from RCL2 to AGND. Refer to Table 3 in the Functional Description section for RCL2 values.

Pin Descriptions (continued)

Pin #	I/O	Name	Function
22	A/I	LVMODE	Local Voltage Mode. When above 1.7V, LVMODE opens the internal Hot-Swap FET to keep the DC-DC controller active. This is a voltage-mode input pin that should be pulled to AGND when not used.
23	A/I	AMPS	Automatic Maintain Power Signature (MPS) amplitude control pin. Connect a resistor from AMPS to AGND to program the MPS current amplitude. Leave AMPS open to disable the automatic MPS function.
24	A/I	MPSD	Maintain Power Signature (MPS) duty cycle set pin. Refer to the applications information to set 12.5%, 8.1% or 5.4% MPS duty cycle operation when used with a type 3 or 4 PSE.
25	O	PST1	PSE Type Indicator 1 Open Drain active-low output. Connect a 10kΩ resistor between this pin and VDD5 for normal operation.
26	O	PST2	PSE Type Indicator 2. Output, Open Drain active-low output. Connect a 10kΩ resistor between this pin and VDD5 for normal operation.
27	O	PSDBT	PSE TYPE 3 or 4 power detect pin for BT operation. Open Drain active-low output. Connect a 10kΩ resistor between this pin and VDD5 for normal operation.
28	A/I	AUT	Auto-class enable input pin. This input is internally terminated to the VDD rail during startup classification. Terminate to AGND to enable the Auto class function during classification. Leave open if not used.
29	A/I	DET	Connect a 25.5kΩ resistor from DET to VIN to provide the PoE detection signature to the PD controller. Terminate DET to GND to disable the pass MOSFET during powered operation.
30	A	AGND	Analog ground pin.
31, 32	P	VOD	Switched supply and Hot Swap Switch output. This pin also serves as the input source for DC/DC controller and VDD10 regulator.
EP	-	Exposed Pad	Local ground. This is the negative output from the external diode bridge and is not isolated from the line input.

I = Input, O = Output, A = Analog Signal, P = Power

Absolute Maximum Ratings[2]

(T_A = 25˚C unless otherwise noted)

Symbol	Description	Value	Units
VIN, VOD, DET	High Voltage Pins	-0.3 to 100	V
VDD10, G1, G2		-0.3 to 16	V
EN/UVLO, VDD5, DT, SS, FREQ, DITHER/SYNC, RCM, FB, COMP, CS, RCURR, RCL1, RCL2, LVMODE, AMPS, MPSD, PST1, PST2, PSDBT, AUT	Low Voltage Pins	-0.3 to 6	V
TS	Storage Temperature Range	-55 to 165	°C
TJ	Die Junction Operating Temperature Range	-40 to 150	°C

ESD and Surge Ratings[3]

Symbol	Description	Value	Units
VESD_HBM	JEDEC JS-001-2017 Human Body Model (HBM)[4]	2	kV
VESD_CDM	JESD22-C101, Charged device model (CDM), All pins	0.5	kV
VESD_CD	IEC61000-4-2 Contact Discharge[5]	8	kV
VESD_AGD	IEC61000-4-2 Air Gap Discharge[5]	15	kV

Thermal Capabilities[6]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	34.4	°C/W
P_D	Maximum Power Dissipation	3.6	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-29.1	mW/°C

Recommended Operating Conditions

Symbol	Description	Min.	Typ.[7]	Max.	Units
$V_{IN-AF\ (Type\ 1\ PD)}$	Input Power Supply	**38**	48	57	V
$V_{IN-BT\ (Type\ 3,4\ PD)}$		42.5	48	57	V
V_{IN-LP}	Local Power Mode (VOD and GND)[8]	9.5		57	V
T_A	Ambient Operating Temperature Range	-40		+85	°C
T_J	Recommended Junction Operating Temperature	-40		+125	°C

2. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
3. ESD and Surge Ratings conform to JEDEC and IEC industry standards. Some pins may actually have higher performance. Surge ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.
4. Human Body Model and Charged Device Model ESD limits are specified at the chip level.
5. Air Discharge, and Contact Discharge are specified at the system level.
6. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
7. Typical specification, not 100% tested. Performance guaranteed by design and/or other correlation methods.
8. Power transformer must be capable of handling the full voltage range.

Electrical Characteristics[9]

Unless otherwise noted, specifications are for T_J = -40°C to +125°C. Typical specifications are for T_J = +25°C and V_{IN} = 48V, Typical specifications not 100% tested.

PD (all PD voltage limits specified at the RJ45 Interface)

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{INRUSH_AF}	Inrush Current Limit (AF) – Type 1 PD	For V_{OUT} ≤ 16V during startup	50	120	240	mA
I_{INRUSH_AT}	Inrush Current Limit (AT) – Type 2 PD	For V_{OUT} ≤ 16V during startup	210	320	400	mA
I_{INRUSH_BT1}	Inrush Current Limit (BT) – Type 3 PD	For V_{OUT} ≤ 16V during startup, (SINGLE-SIGNATURE)	300	410	500	mA
I_{INRUSH_BT2}	Inrush Current Limit (BT) – Type 4 PD	For V_{OUT} ≤ 16V during startup, (SINGLE-SIGNATURE)	380	530	630	mA
I_{IN_AF}	Operating Current – Type 1	R_{CURR} = GND; device configured for 13W operation			450	mA
I_{IN_AT}	Operating Current – Type 2	R_{CURR} = 5kΩ, device configured for 30W operation			750	mA
I_{IN_BT1}	Operating Current – Type 3	R_{CURR} = 10kΩ; device configured for 60W operation			1500	mA
I_{IN_BT2}	Operating Current – Type 4	R_{CURR} = left open; device configured for 90W operation			2000	mA
$I_{LIM\text{-}AF}$	PoE Current Limit– Type 1	R_{CURR} = GND; device configured for 13W operation	450	600		mA
$I_{LIM\text{-}AT}$	PoE Current Limit – Type 2	R_{CURR} = 5kΩ device configured for 30W operation	750	1000		mA
$I_{LIM\text{-}BT1}$	PoE Current Limit– Type 3	R_{CURR} = 10kΩ; device configured for 60W operation	1500	1800		mA
$I_{LIM\text{-}BT2}$	PoE Current Limit– Type 4	R_{CURR} = left open; device configured for 90W operation	2000	2500		mA
$R_{DS\text{-}ON}$	Hot-Swap FET On Resistance	I_{IN} = 2A		0.13	0.2	Ω
V_{DET_MIN}	Min Detection Signature voltage				2.7	V
V_{DET_MAX}	Max Detection Signature voltage		10.1	12.5	14.5	V
V_{CL_LOW}	Classification Lower Threshold	V_{IN} Rising, Classification turn on	11.0	12.5	14.5	V
$V_{CL\_LOW\_HY}$	Classification lower threshold hysteresis			1.4		V
V_{CL_HIGH}	Classification Upper Threshold	V_{IN} Rising, Classification turn off	20.5	22.0	25	V
$V_{CL\_HIGH\_HY}$	Classification Upper Threshold hysteresis			1.1		V
V_{MARK_MIN}	Min Mark Event Voltage				6.9	V
V_{MARK_MAX}	Max Mark Event Voltage		10.0	12.5	13.0	V
V_{CLMK_HYS}	Classification-Mark Hysteresis			1.5		V
V_{CL_RST}	Classification Reset Voltage		2.8		6.90	V
$I_{CLASS\_}$	Classification Current: signature 0 (RCL to VDD5 or NC)	For Voltage classification range: 12.5 < V_{CL} < 20.5	1		4	mA
	Classification Current: signature 1 (RCL = 280K)		9		12	
	Classification Current: signature 2 (RCL = 143K)		17		20	
	Classification Current: signature 3 (RCL = 90.9K)		26		30	
	Classification Current: signature 4 (RCL = 63.4k)		36		44	
$V_{IN\_UVLO\_R}$	Input UVLO Threshold	V_{IN} Rising	35.8	38	42	V
$V_{IN\_UVLO\_F}$		V_{IN} Falling	30	32	34	
T_{FLC}	First long class event timing		75.5	81.5	87.5	ms

9. It is guaranteed to meet performance specifications over the –40°C to +125°C operating Junction temperature range by design, characterization and correlation with statistical process controls.

Electrical Characteristics (continued)[10]

Unless otherwise noted, specifications are for T_J = -40°C to +125°C. Typical specifications are for T_J = +25°C and V_{IN} = 48V, Typical specifications not 100% tested.

Detection Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
R_{DET}	Detection Resistance		23.8	25.5	26.0	KΩ
V_{DOF}	Detection offset voltage				0.6	V

Maintain Power Signature (MPS) Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{MPSF}	MPS Current Enable Threshold	Load current falls to enable MPS current		30		mA
I_{MPSR}	MPS Current Disable Threshold	Load current rises to disable MPS current		35		
R_{AMPS}	Resistance options on AMPS pin to GND to program the MPS current amplitude.	R_{AMPS} = 237kΩ		10		mA
		R_{AMPS} = 150kΩ		16		
		R_{AMPS} = 118kΩ		20		

Local Power Mode Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{LV}	LVMODE Threshold LOW			1.2	1.3	V
V_{HV}	LVMODE Threshold HIGH		1.6	1.7		V

EN/UVLO Pin Threshold Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
EN	En Threshold	V_{EN} Rising		1.2		V
EN_H	En Hysteresis			150		mV

Feedback (FB)

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{FB}	FB Pin Voltage		1.176	1.2	1.224	V

VDD5 Internal Regulator

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{VDD5}	5V Regulator Output Voltage	C_{VDD5} = 1µF		4.7		V

VDD10

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{VDD10}[11]	10V regulator Output Voltage	VIN = 48, I_{VDD10} = 1mA, C_{VDD10} = 1µF	9	10	11.5	V
I_{VDD10}	Supply current			20		mA

10. Specification guaranteed to meet performance specifications over the –40°C to +125°C operating Junction temperature range by design, characterization and correlation with statistical process controls.

11. VDD10 provides bias for the internal gate drive.

Electrical Characteristics (continued)[12]

Unless otherwise noted, specifications are for T_J = -40°C to +125°C. Typical specifications are for T_J = +25°C and V_{IN} = 48V, Typical specifications not 100% tested.

Ramp/Slope Compensation

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{SLOPE}	Slope Bias Current of RCM pin			10		µA
S_{AVC}	Slope Compensation ramp at Sense Input			1.8		mV/ (µs*kΩ)

Error Amplifier

Symbol	Description	Conditions	Min	Typ	Max	Units
GBW	Gain Bandwidth			10		MHz
A_{CC}	DC Gain			65		dB
A_{GM}	Transconductance	V_{FB} = 1.24V, V_{COMP} = 1V	80	120	150	µS

General

Symbol	Description	Conditions	Min	Typ	Max	Units
Vcomp	Level shift between comp node and PWM comparator			-800		mV
Vref	Cycle skipping threshold at comparator			200		mV
Rpullup	Internal pullup on comp node	FB = GND		1		MΩ
		FB > VDD5-1V		3.1		kΩ
D	Duty cycle				80	%

Current Limit/Protection

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{CSD}	Current limit threshold		240	300	340	mV

Soft-Start/Soft Stop (SS)

Symbol	Description	Conditions	Min	Typ	Max	Units
I_{SSC}	Soft start charger current			10		µA
I_{SSD}	Soft-stop Dis-charger current			10		µA

Dithering Ramp Generator

Symbol	Description	Conditions	Min	Typ	Max	Units
$I_{DITHERC}$	Charging Current			50		µA
$I_{DITHERD}$	Discharging Current			50		µA
V_{RH}	Ramp High Trip			2		V
V_{RL}	Ramp Low Trip			0.4		V

Oscillator (FREQ)

Symbol	Description	Conditions	Min	Typ	Max	Units
F_{SW}	Freq Adjustable Range		75	150	1000	KHz
F_{SW_Tol}	Freq Tolerance			±10%		
D_{MAX}	Maximum duty cycle	VIN = 48V, DT = 0nS		82		%

12. Specification guaranteed to meet performance specifications over the –40°C to +125°C operating Junction temperature range by design, characterization and correlation with statistical process controls.

Electrical Characteristics (continued)[13]

Unless otherwise noted, specifications are for T_J = -40°C to +125°C. Typical specifications are for T_J = +25°C and V_{IN} = 48V, Typical specifications not 100% tested.

External Sync Input (DITHER/SYNC)

Symbol	Description	Conditions	Min	Typ	Max	Units
SYNC	SYNC Input Threshold	V_{SYNC} Rising		2.9		V

Gates Driver

Symbol	Description	Conditions	Min	Typ	Max	Units
T_R	Rise Time	C_{LOAD} = 2.0nF, VDD = 10V		15		ns
T_F	Fall Time	C_{LOAD} = 2.0nF, VDD = 10V		15		ns
	Peak current Source			1.5		A
	Peak current Sink			1.5		A

Thermal Protection Specifications

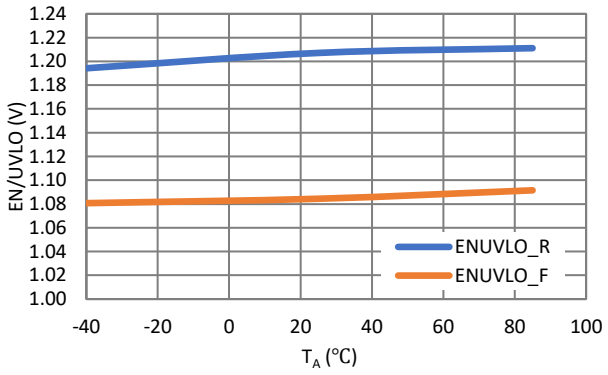
Symbol	Description	Conditions	Min	Typ	Max	Units
T_{J_TS}	Thermal Shutdown Temperature			160		°C
T_{J_HYS}	Thermal Shutdown Hysteresis			30		°C

13. Specification guaranteed to meet performance specifications over the –40°C to +125°C operating Junction temperature range by design, characterization and correlation with statistical process controls.

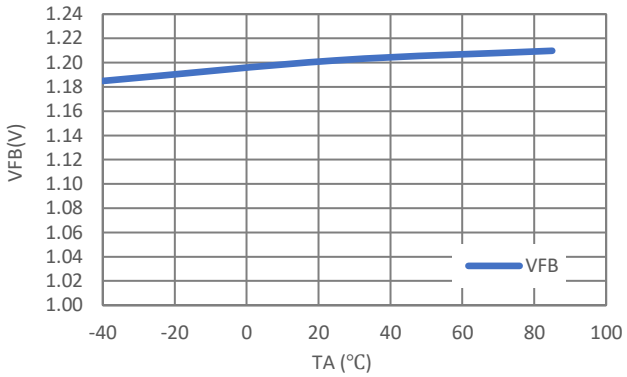
Typical Characteristics

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 6A, Downstream DC-DC with Active clamp Forward Circuit topology, T_A = 25°C, unless otherwise specified.

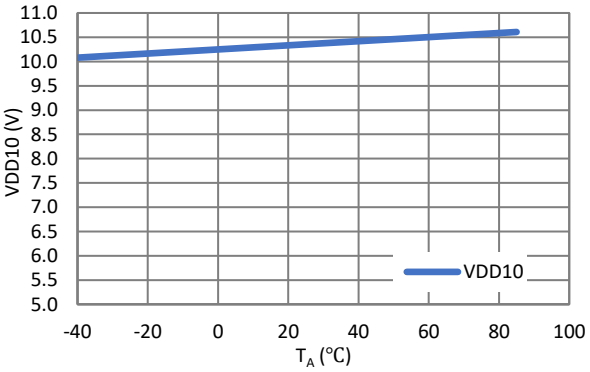
EN/UVLO vs. Temperature



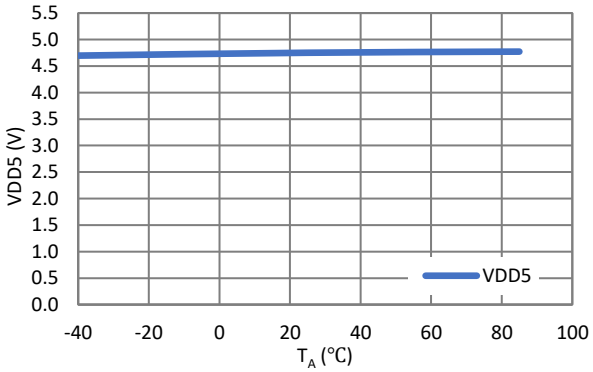
VFB vs. Temperature



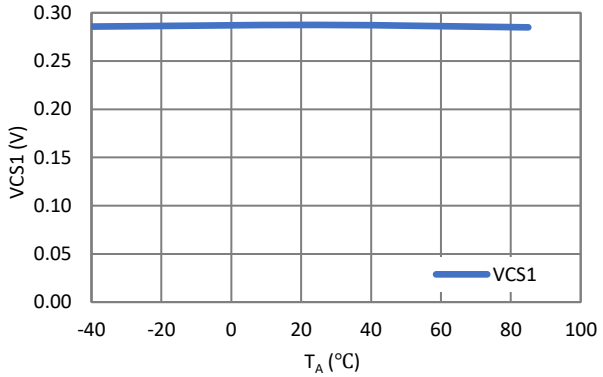
VDD10 vs. Temperature



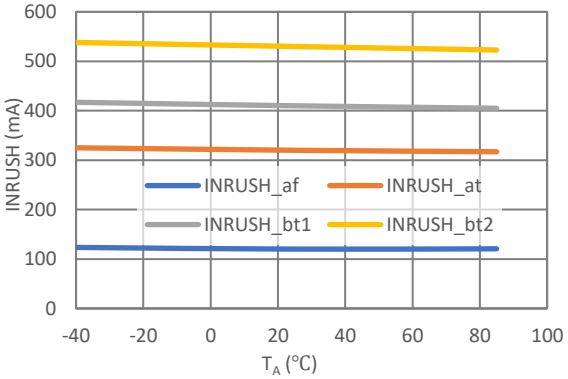
VDD5 vs. Temperature



VCS1 vs. Temperature



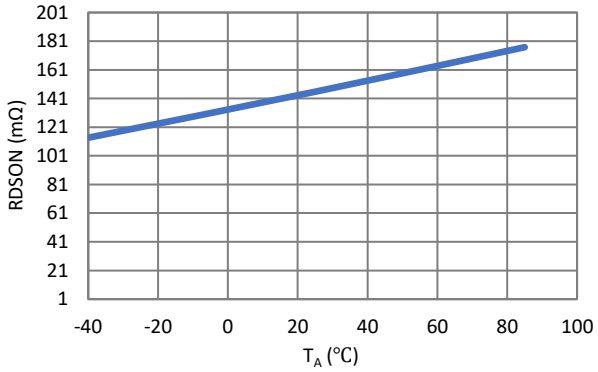
Inrush vs. Temperature



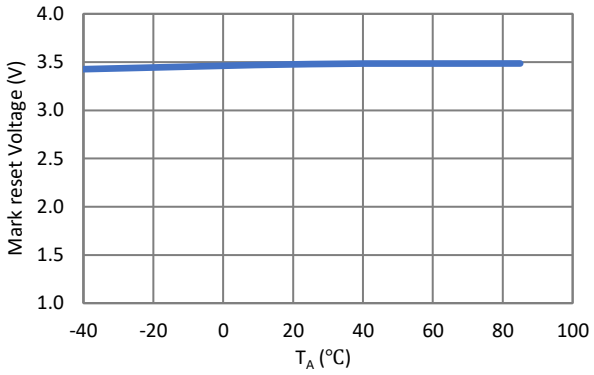
Typical Characteristics (continued)

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 6A, Downstream DC-DC with Active clamp Forward Circuit topology, T_A = 25°C, unless otherwise specified.

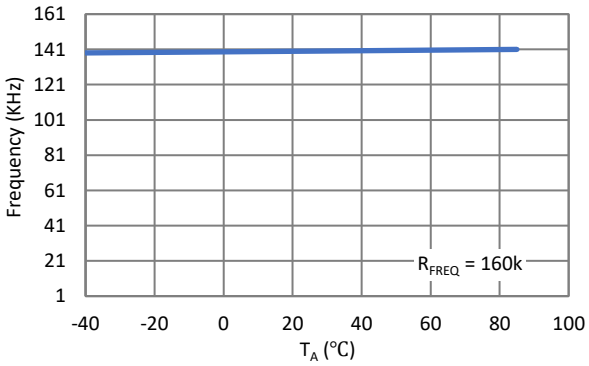
Hot-Swap FET R_{DSON} vs. Temperature



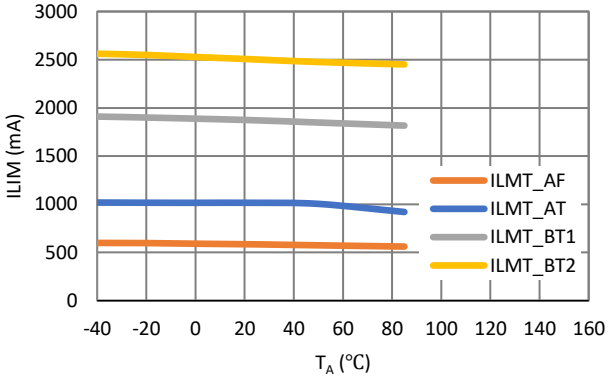
Mark Reset Voltage vs. Temperature



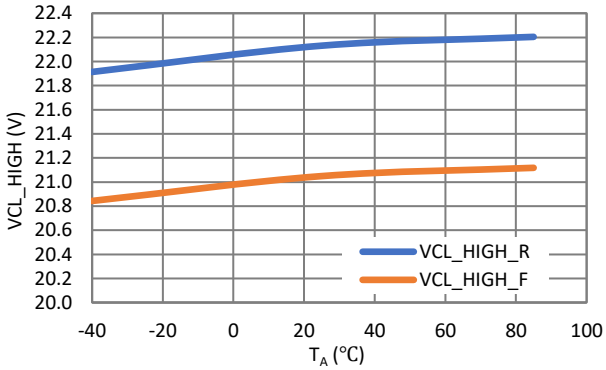
Frequency vs. Temperature



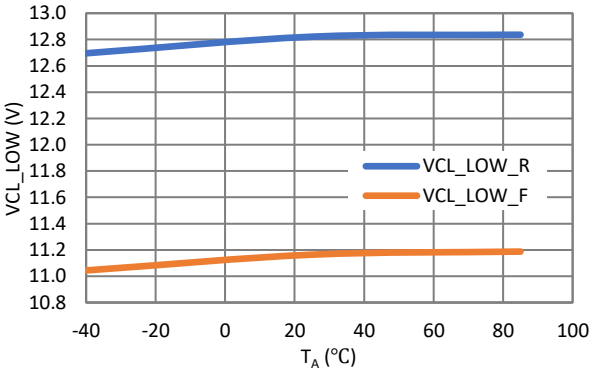
PD Current LIMIT vs. Temperature



Classification Upper Threshold vs. Temperature



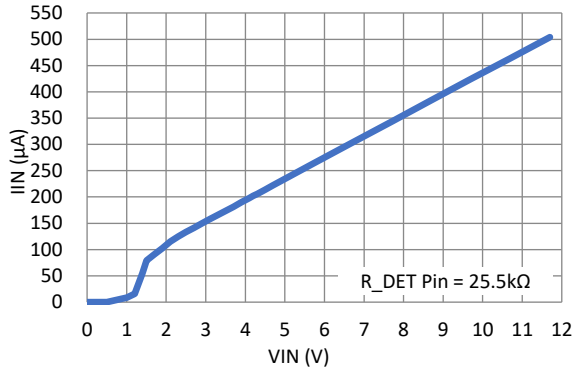
Classification Lower Threshold vs. Temperature



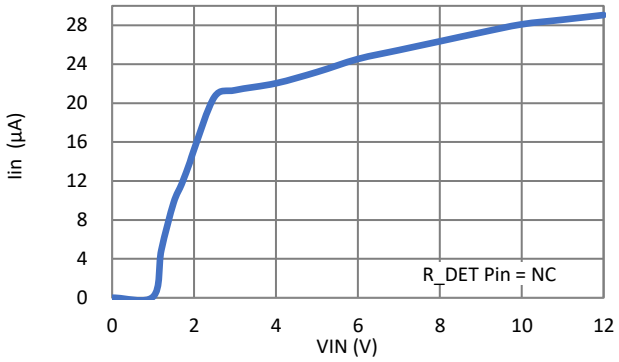
Typical Characteristics (continued)

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 6A, Downstream DC-DC with Active clamp Forward Circuit topology, T_A = 25°C, unless otherwise specified.

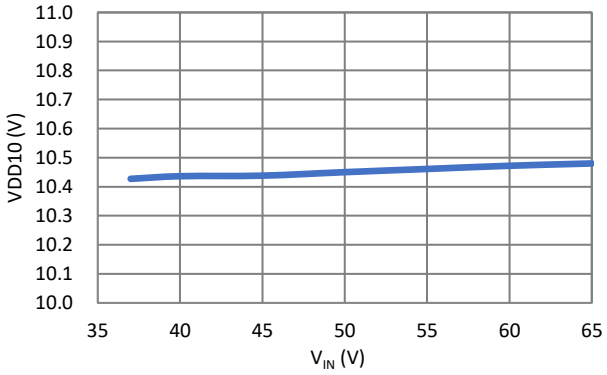
Detection Current vs. Input Voltage



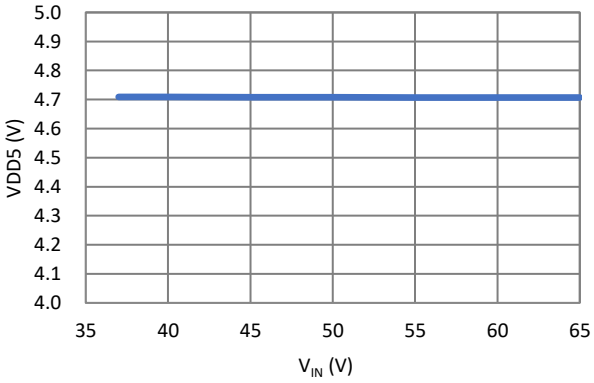
Quiescent Current vs. Input Voltage



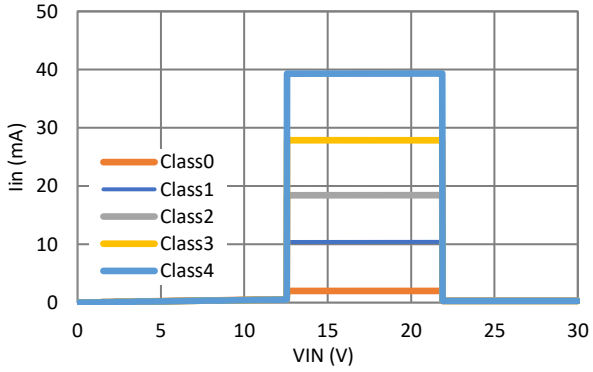
VDD10 vs. V_{IN}



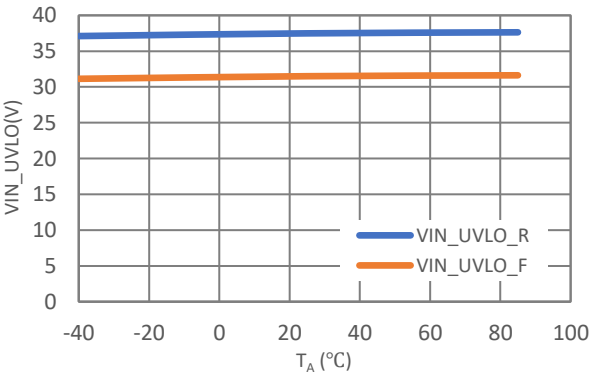
VDD5 vs. V_{IN}



Classification Current vs Input Voltage



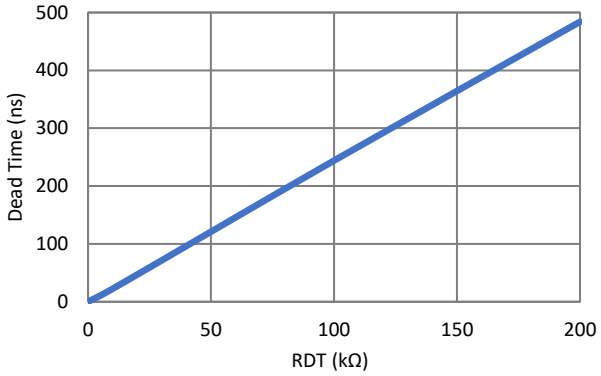
V_{IN_UVLO} vs. Temperature



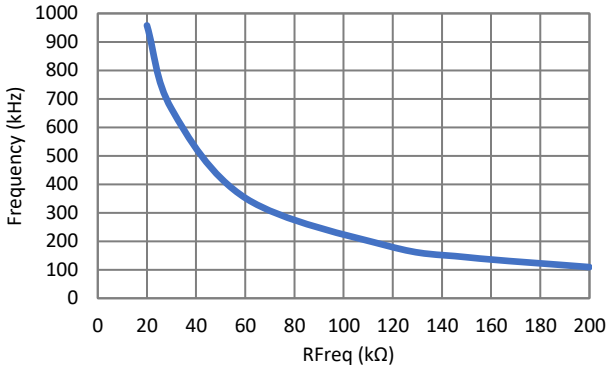
Typical Characteristics (continued)

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 6A, Downstream DC-DC with Active clamp Forward Circuit topology, T_A = 25°C, unless otherwise specified.

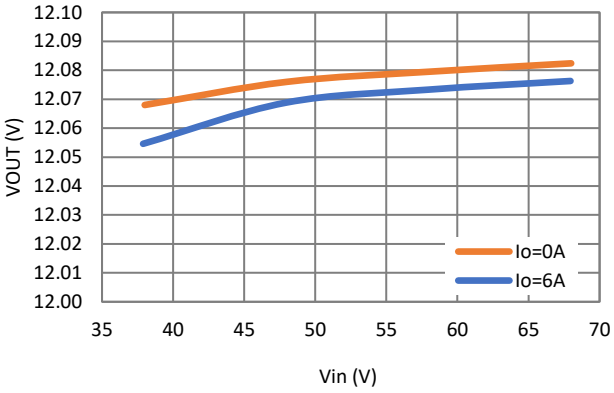
Dead Time vs. Programming Resistance



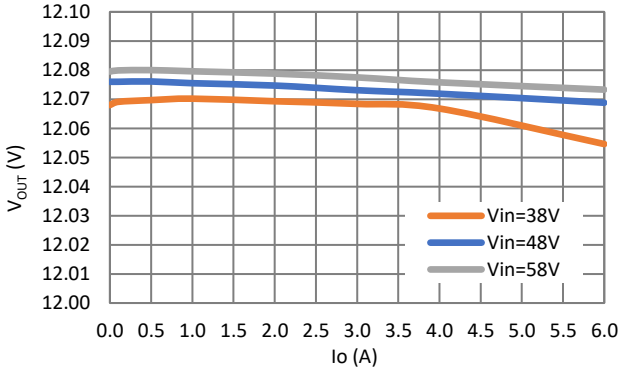
Switching Freq. vs. Programming Resistance



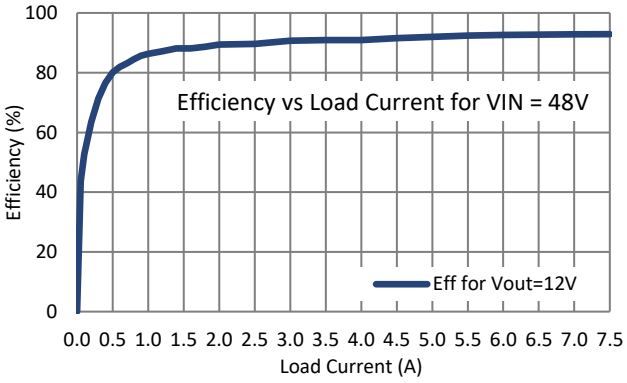
Line Regulation



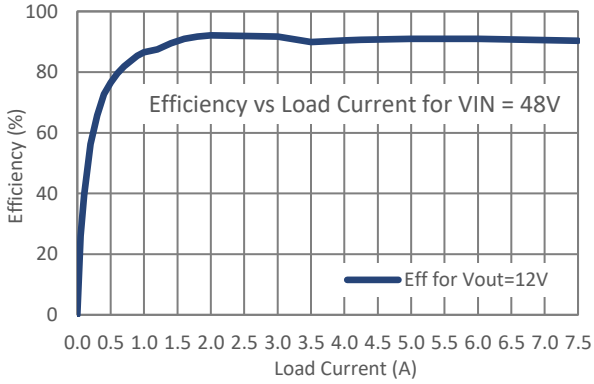
Load Regulation



Efficiency vs Load Current
Forward with Synchronous Secondary Topology



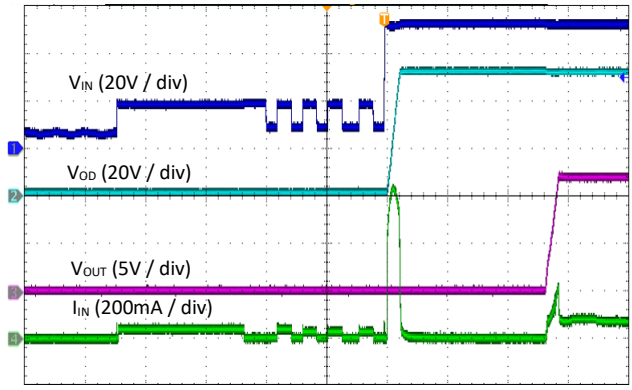
Efficiency Vs Load Current
Flyback with Synchronous Secondary Topology



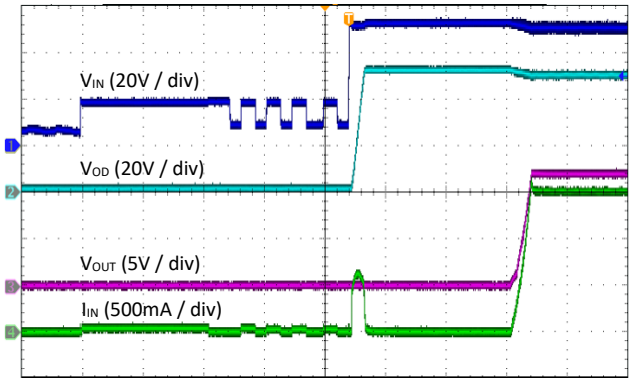
Typical Characteristics (continued)

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 6A, Downstream DC-DC with Active clamp Forward Circuit topology, T_A = 25°C, unless otherwise specified.

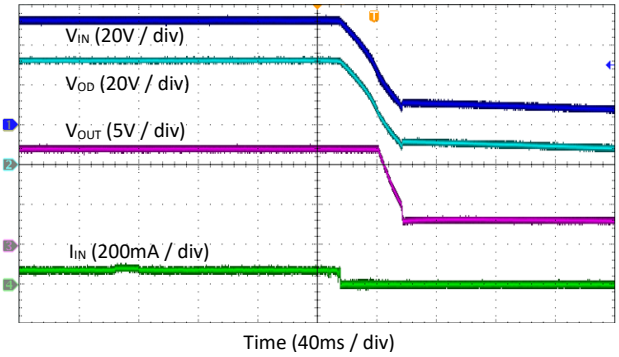
Startup with PSE Input at Downstream 12V-0A Load



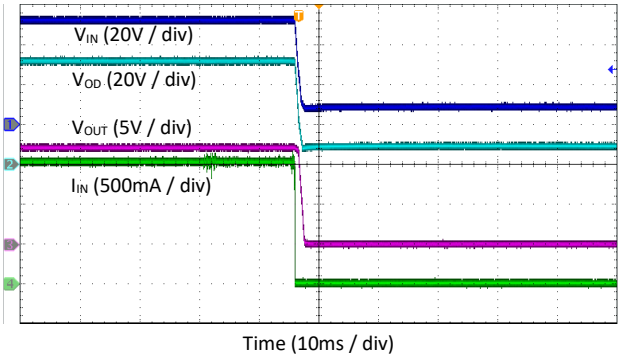
Startup with PSE Input at Downstream 12V-6A Load



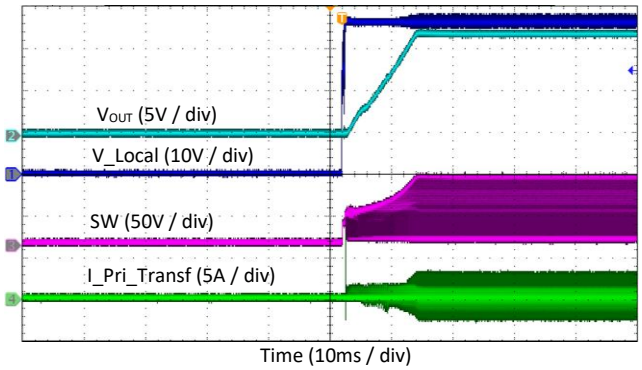
Shutdown by PSE at Downstream 12V-0A Load



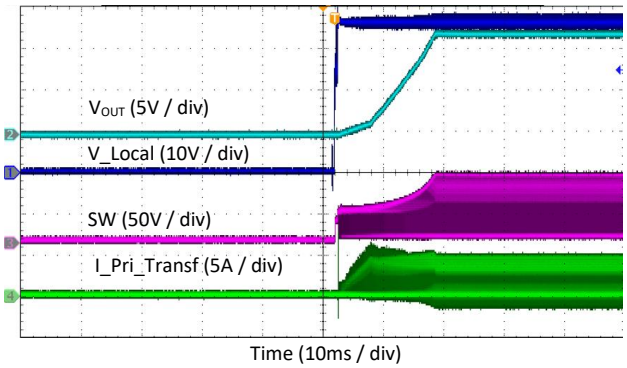
Shutdown by PSE at Downstream 12V-6A Load



Startup with Local Power at Downstream 12V-0A Load



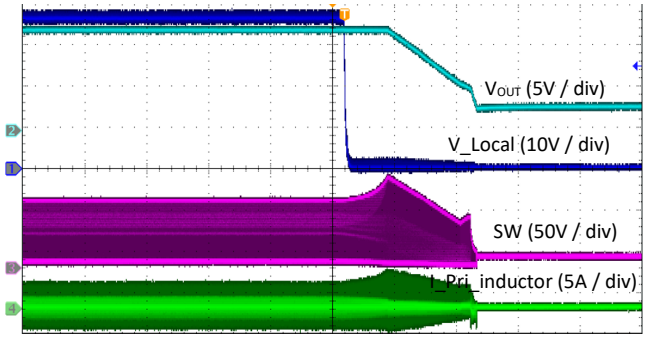
Startup with Local Power at Downstream 12V-6A Load



Typical Characteristics (continued)

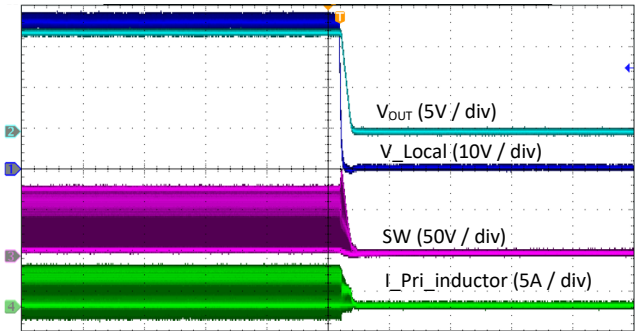
V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 6A, Downstream DC-DC with Active clamp Forward Circuit topology, T_A = 25°C, unless otherwise specified.

Shutdown with Local Power at Downstream 12V-0A Load



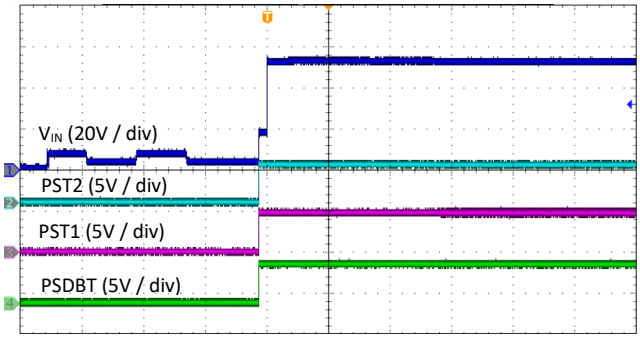
Time (10ms / div)

Shutdown with Local Power at Downstream 12V-6A Load



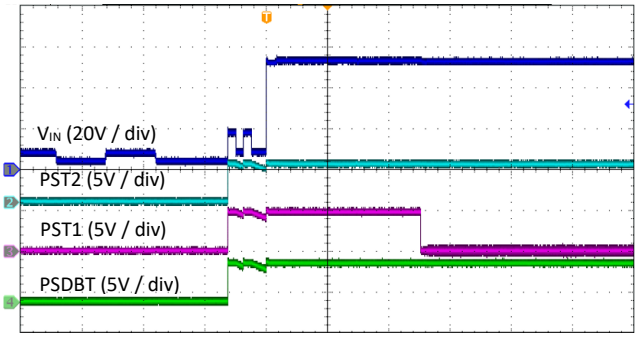
Time (10ms / div)

PSDBT PST Detect at PD Class0-3, af/at PSE



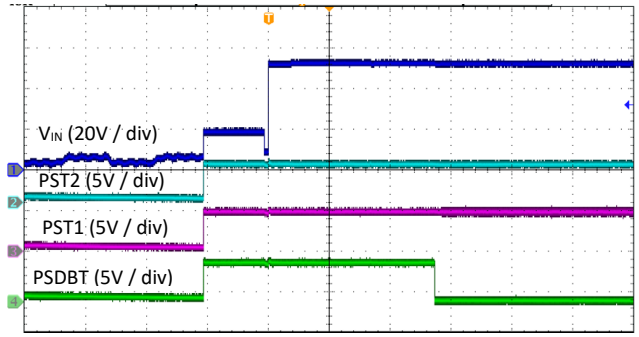
Time (100ms / div)

PSDBT PST Detect at PD Class4, af/at PSE



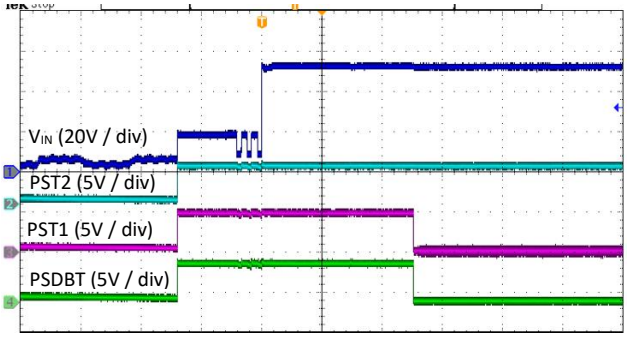
Time (100ms / div)

PSDBT PST Detect at PD Class0-3, bt PSE



Time (100ms / div)

PSDBT PST Detect at PD Class4, bt PSE

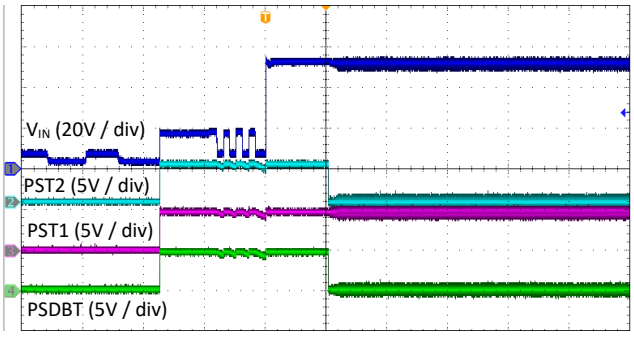


Time (100ms / div)

Typical Characteristics (continued)

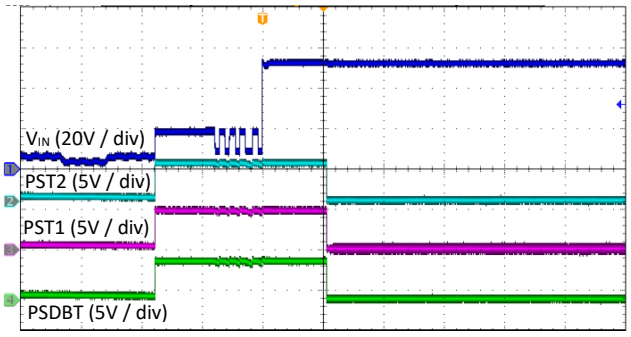
V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 6A, Downstream DC-DC with Active clamp Forward Circuit topology, T_A = 25°C, unless otherwise specified.

PSDBT PST Detect at PD Class5-6, bt PSE



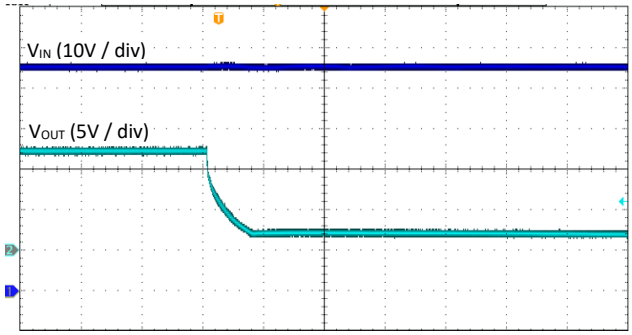
Time (100ms / div)

PSDBT PST Detect at PD Class7-8, bt PSE



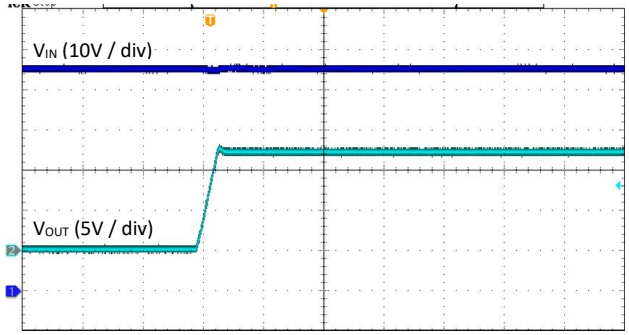
Time (100ms / div)

Over Temperature Protection



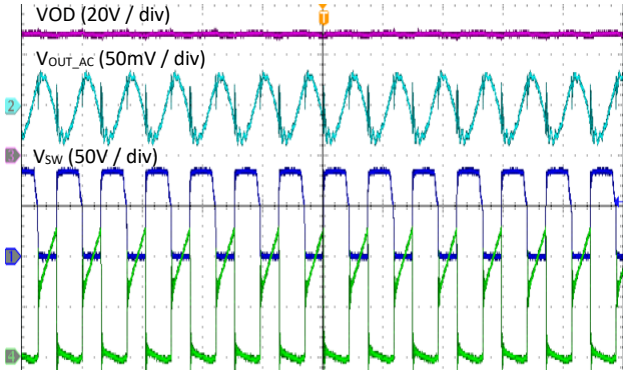
Time (20ms / div)

Over Temperature Protection Restart



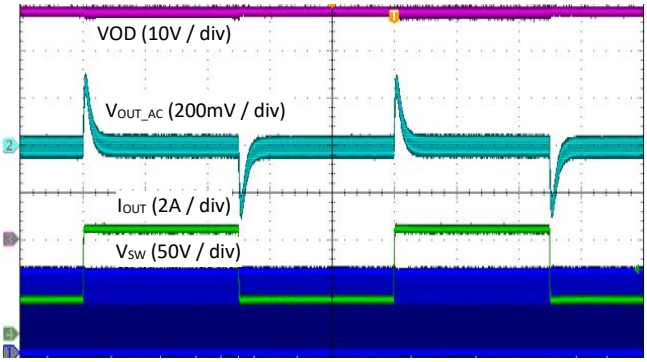
Time (20ms / div)

Steady State Switching (12V-6A load)



I_Primary-Transform (2A / div)

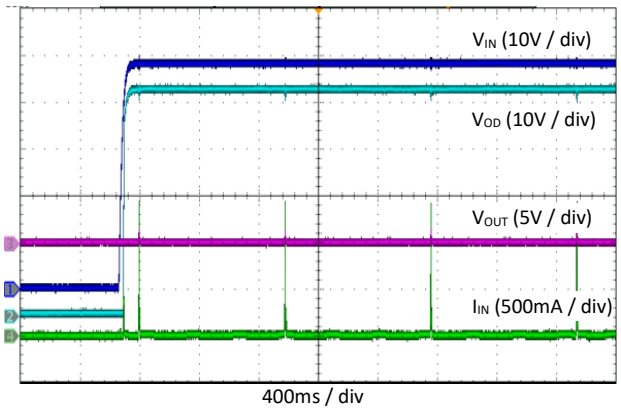
Transient Load Response (1.5A-4.5A load)



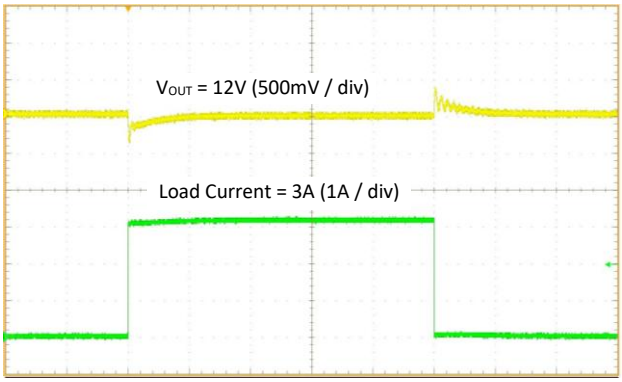
Typical Characteristics (continued)

V_{IN} = 48V, V_{OUT} = 12V, I_{OUT} = 6A, Downstream DC-DC with Active clamp Forward Circuit topology, T_A = 25°C, unless otherwise specified.

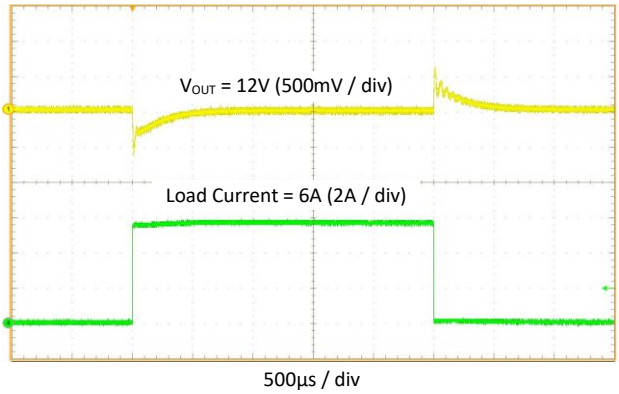
V_{OUT} Short Protection



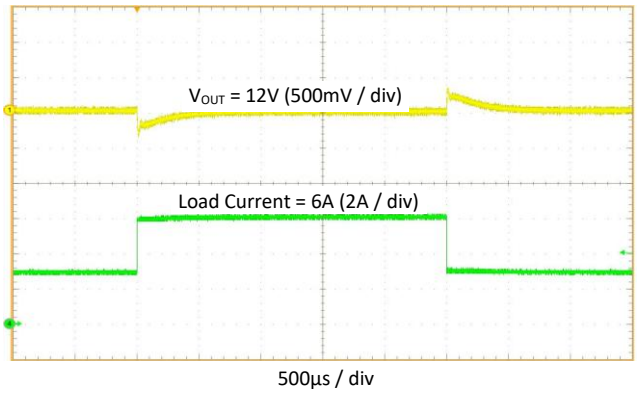
Load Transient Response (0A to 3A)



Load Transient Response (0A to 6A)



Load Transient Response (3A to 6A)



Functional Block Diagram

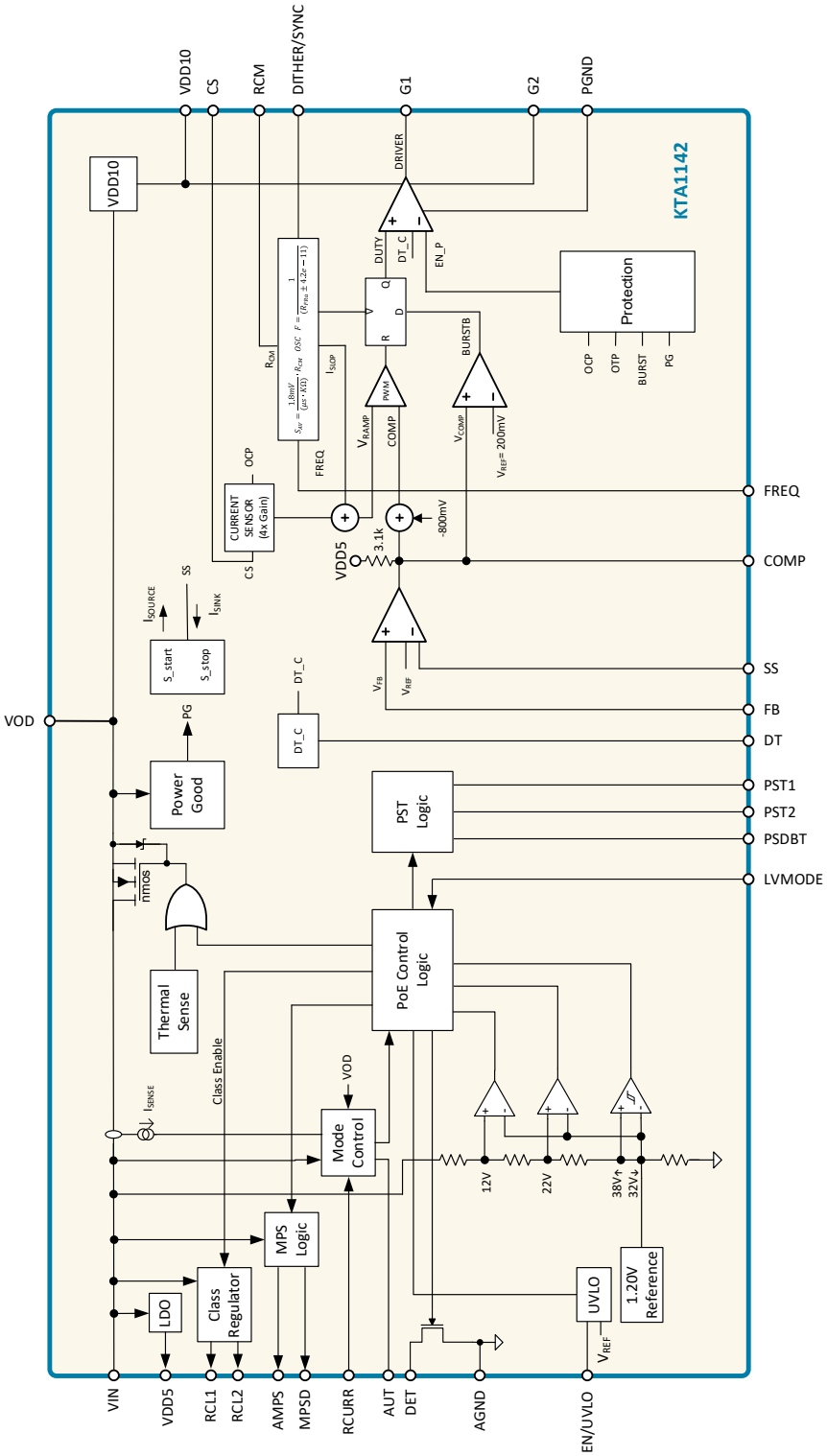


Figure 1. Functional Block Diagram

Functional Description

Overview of PoE

Power over Ethernet (PoE) offers an economical alternative for powering end network appliances, such as IP telephones, wireless access points, security and web cameras, and other powered devices (PDs). PoE standards IEEE® Std. 802.3af, 802.3at and 802.3bt are intended to unify the delivery method of usable power over Ethernet cables to remotely powered client devices. These standards define a method for detecting and querying PDs and then supplying a range of current levels based on the power class the device belongs to. By employing this method, designers can create systems that predict and minimize power usage, allowing the maximum number of devices to be supported on a powered Ethernet network.

The power source that provides current through the Ethernet cables to remote devices is referred to as the Power Sourcing Equipment (PSE). The powered device (PD) on the other end of the Ethernet cable negotiates for and receives the agreed-upon power. IEEE® Std. 802.3af limits PSE power delivery to <13W at the PD input (Type 1 PD). IEEE® 802.3at allows for >13W power levels and up to <25.5W (Type 2 PD). There are two higher power levels in the IEEE® 802.3bt standard that limits PSE power delivery to <51W (Type 3 PD) and <71.3 (Type 4 PD) at the PD input.

Table 1. Classification Settings for PoE Power Device

PD Requested Class	Standard	PD Power (Watt)	PSE Power (Watt)	PD Type	Max Number of Events	2 or 4 Pair Power	Auto Class
0	802.3af	12.95	15.4	1	-	2 or 4 Pair	NO
1	802.3af	3.84	4	1	1	2 Pair Only	NO
2	802.3af	6.49	7	1	1	2 Pair Only	NO
3	802.3af	12.95	15.4	1	1	2 or 4 Pair	NO
4	802.3at	25.5	30	2	2	2 or 4 Pair	NO
5	802.3bt	38.25	45	3	4	4 Pair Mandatory	Optional
6	802.3bt	51	60	3	4	4 Pair Mandatory	Optional
7	802.3bt	62	75	4	5	4 Pair Mandatory	Optional
8	802.3bt	71.3	90	4	5	4 Pair Mandatory	Optional

The PSE uses the following sequence to detect a connected PD, determine how much power it requires and then initiate supply current to the device:

1. **Reset** — Power is withdrawn from the PD if the applied voltage falls below a specified level.
2. **Signature Detection** — The PSE detects and evaluates whether the PD is a valid PoE device.
3. **Classification** — The PSE reads the power requirement of the PD. The Classification level identifies how much power the PD will require from the Ethernet line. This permits optimum use of the total power available from the PSE.
4. **On** — Operational state, during which the PSE provides the allocated power level to the PD.

This sequence occurs as a progressively rising voltage level from the PSE. It is designed to prevent high voltages from being present on an Ethernet line that does not have a valid PD attached (for user and non-PoE device safety).

To design PoE systems according to IEEE® standards, the following constraints apply listed in Table 2:

Table 2. PoE Requirements

Requirement	Value
Input voltage at Type 1 PD interface	37V-57V
Input voltage at Type 2 PD interface	42.5V-57V
Input voltage at Type 3 PD interface	42.5V-57V
Input voltage at Type 4 PD interface	41.1V-57V
Output voltage from Type 1 PSE	44V-57V
Output voltage from Type 2 PSE	50V-57V
Output voltage from Type 3 PSE	50V-57V
Output voltage from Type 4 PSE	52V-57V
Minimum operating current limit, Type 1 @ PSE min output voltage	350mA
Minimum operating current limit, Type 2 @ PSE min output voltage	600mA
Minimum operating current limit, Type 3 @ PSE min output voltage	600mA per pair
Minimum operating current limit, Type 4 @ PSE min output voltage	960mA per pair

KTA1142 Detailed Overview

The KTA1142 is a fully integrated PD device with DC-DC controller that provides the functionality required for Power-over-Ethernet (PoE) applications with Active Clamp control of isolated DC/DC solutions in Flyback or Forward converter circuit configurations. The optimized architecture reduces external component cost with a minimized solution footprint while delivering high performance.

To meet PoE standards requirements, the KTA1142 includes a fully integrated PoE PD controller for Type1-4 PD implementations. The KTA1142 meets all system requirements for the IEEE® 802.3 standard for Ethernet and all power management requirements for the IEEE® standard 802.3bt-2018 standard.

The KTA1142 acts as an interface to the PSE, performing all detection, classification, and inrush current limiting control necessary for compliance with the PoE standards. An internal MOSFET and control circuit limits the inrush and steady-state current drawn from the Ethernet line. External rectification bridges protect against input polarity reversal and provides alternative input power detection.

The KTA1142 passes 8kV Contact Discharge and 15kV Air Discharge requirements, tested per IEC 61000-4-2. EMI compliance of KTA1142-based designs has been verified for CISP22 and FCC Class-B radiated and conducted emissions.

Rectification and Protection

To protect against input supply polarity reversal, an external Rectification bridge is required. In conjunction with the external bridge, the KTA1142 provides over-voltage and transient protection on the line side of the Hot-Swap FET.

The KTA1142 is implemented using a robust 100V process technology. By integrating high voltage input protection circuitry, the device is able to provide fast response to surge events. The design also limits stray surge current from passing through sensitive circuits, such as the Ethernet PHY device and enables low-impedance safe discharge path directly to the local ground. The protection circuit has been carefully designed to ensure that during these surge events, where currents can reach as high as 30A, the circuit voltage does not exceed critical breakdown limits, protecting the PD from damage by the event. This technology also enables system designers to achieve 15kV/8kV Air/Contact Discharge ESD performance.

PD Controller

The KTA1142 PD Control Interface is designed to provide full PD functionality for IEEE® 802.3af/at/bt compliant systems, with programmable support for standard PD control functions.

The PD Controller provides the following major functions:

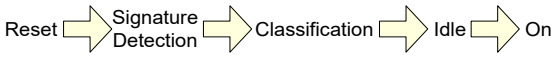
- A resistance/capacitance connection path for the detection signature.
- Classification current for power classification.
- Type 4 (Class 8) Power capability for PD supply
- Power management and thermal protection shutdown, including UVLO (Under Voltage Lock Out).
- PSE type indicator output signal pins
- BT PSE detection output pin, active when a BT PSE source can provide more than 30 watts.
- 5 Event Physical Layer classification.

Modes of Operation

The KTA1142 has five operating modes:

1. **Reset** — All device functions are disabled
2. **Detection** — the external PD detection signature resistance / capacitance components are applied across the input.
3. **Classification** — PD indicates power requirements to the PSE via the VIN start-up signature number of events for classification of IEEE® 802.3af/at/bt
4. **Idle** — Standby state is entered after Classification and remains in standby until the full-power input voltage is applied by the PSE.
5. **On** — The PD is enabled and supplies power to the DC-DC controller and the local application circuitry.

As the supply voltage from the PSE increases from 0V, the KTA1142 transitions through the modes of operation in this sequence:



If no PSE or local power supply is present, the line voltage will be zero which will place the KTA1142 in the Reset state. The KTA1142 will not affect Ethernet data link functions.

Reset

When the voltage supplied to the KTA1142 drops below the minimum valid detection voltage (i.e. <2.7V), the device will enter the Reset state. While in Reset, the power supply to the PD is disconnected. The KTA1142 consumes minimal power and the device will revert to the pre-detection state.

Detection Mode

During the detection sequence, the PSE periodically applies a voltage to the PD to read its detection signature. The reading of the signature determines if a PD is present.

During detection, the PSE applies two sequential voltage levels, 1V or more apart and within the detection voltage range of 2.7V to 10.1V. The PSE controller extracts a detection signature resistance value from an incremental I-V slope of the applied signal. Valid I-V slope resistance values range between 23.75kΩ and 26.25kΩ.

With the KTA1142, detection signature resistance is generated by an external resistor connected between VIN and GND on DET Pin. Typically, this is a 25.5kΩ, 1% resistor. With this value of RSIGNATURE, the PSE normally

detects a total effective signature resistance of approximately 25kΩ, which is within the 802.3af/at/bt specification range of 23.75kΩ to 26.25kΩ.

Valid PD detection also requires a valid detection signature capacitance of 0.05µF to 0.12µF at 2.7V to 10.1V with a 1.9V maximum offset voltage per the IEEE® 802.3bt standard as measured at the PD input connector. KTA1142 detection signature capacitance is generated by an external 68nF capacitor connected between VIN and GND. The offset voltage is mainly provided by the external bridge voltage drop.

Classification Mode

Each class represents a power allocation range for a PD to assist the PSE in managing power distribution. IEEE® Std. 802.3bt defines classes of power levels for PDs, listed in Table 1. The KTA1142 supports IEEE® . 802.3af/at and 802.3bt standards for up to 5 Event Physical Layer classifications, as shown in Figure 2 and Figure 3.

In real applications, noise or transient ringing on the ethernet data lines during the classification phase can lead to false classification events or PSE type detection. To prevent incorrect classification events, the KTA1142 integrates a proprietary digital filtering to reduce the effects of line noise for as long as 100µS during the classification phase to ensure reliable BT Detection.

KTA1142 allows the system designer to program the classification current via external resistors. Each of the two external resistors connected between RCL1 and RCL2 pins and ground provide a distinct classification signature to the PSE. The classification signature is then used to define the power class requested by the PD.

The current drawn by each resistor, combined with internal KTA1142 circuit leakage current creates the classification signature current. The number of classification cycles then determines how much power is allocated by the PSE. The power level and programming resistor values for each class are shown in Table 3. For Class 0, the RCL1 and RCL2 pins need to be pulled up to VDD5. This can be a direct short to VDD5 or using a pull-up resistor value up to 100kΩ.

Use Equation 1 to determine the typical classification current:

$$I_{Class}\,[mA] = 2.0 + \frac{2360}{R_{Class}[k\Omega]} \qquad \text{Equation 1}$$

Tolerance = Maximum of ±1.8mA or ±9%

Once the classification process is done, the PD disables the classification current to conserve power.

Table 3. Classification Settings Resistors Selection in RCL1 and RCL2 Pins

PD Class	PD Type	Power (W)	Class 1 Signature	Class 2 Signature	Number of Class Events for Max Power	R_{CL1} (kΩ), 1%	R_{CL2} (kΩ), 1%
0	1	0.44-12.95	0	0	1	Pull-up (0-100kΩ) to VDD pin	Pull-up (0-100kΩ) to VDD5 pin
1	1	0.44-3.84	1	1	1	280	280
2	1	3.84-6.49	2	2	1	143	143
3	1	6.49-12.95	3	3	1	90.9	90.9
4	2	12.96-25.5	4	4	2,3	63.4	63.4
5	3	25.5-38.25	4	0	4	63.4	Pull-up (0-100kΩ) to VDD5 pin
6	3	38.25-51	4	1	4	63.4	280
7	4	51-62	4	2	5	63.4	143
8	4	62-71.3	4	3	5	63.4	90.9

Idle Mode

After the classification process, the PD enters Idle mode while it waits for On-state power delivery from the PSE. PD Current usage is limited to monitoring circuitry to detect the On-state voltage threshold.

On State

In the On State, the KTA1142 supplies power from across the Ethernet line(s) to the PD. The PD enables power to the KTA1142 DC-DC converter stages to then power the downstream PoE system.

PoE Power-On Startup Waveform

Figure 2 represents the power-on sequence for PoE af operation with event voltage level tolerances. Figure 3 represents higher power levels up to a 5-classification event power-on sequence for PoE bt operation. These waveforms reflect typical voltages present at the PD during signature, classification and power-on sequences.

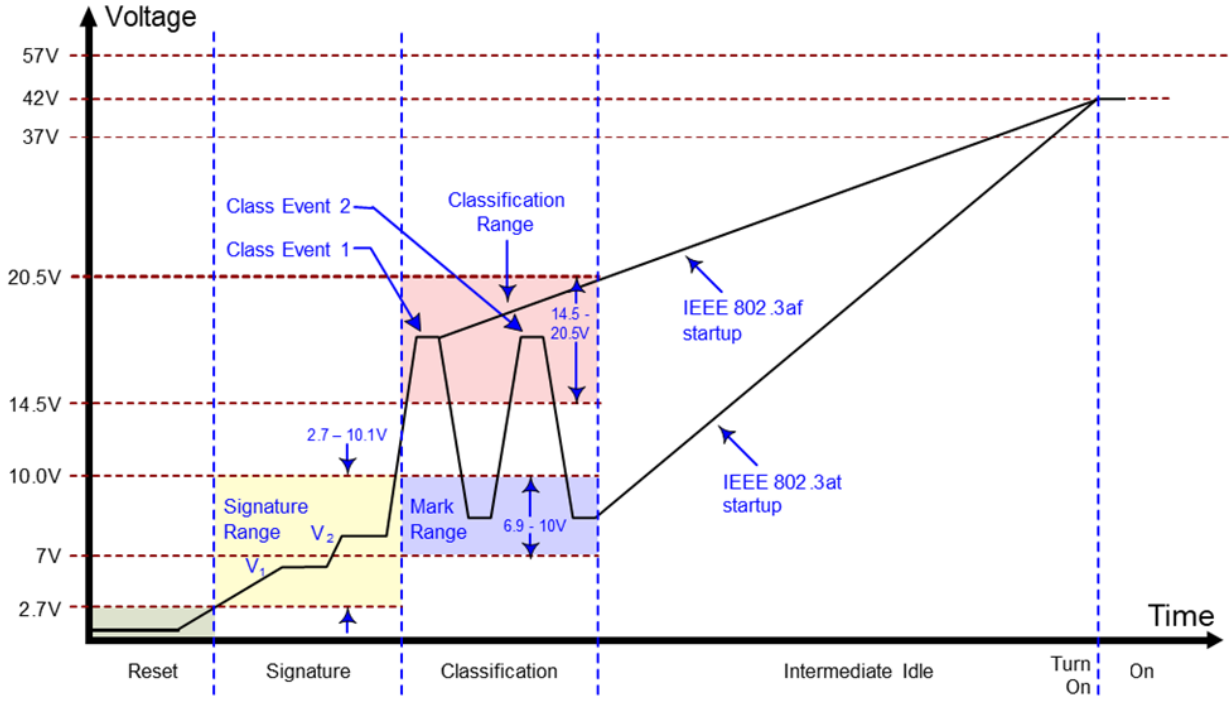


Figure 2. IEEE 802.3af/at Typical Power-On Waveform

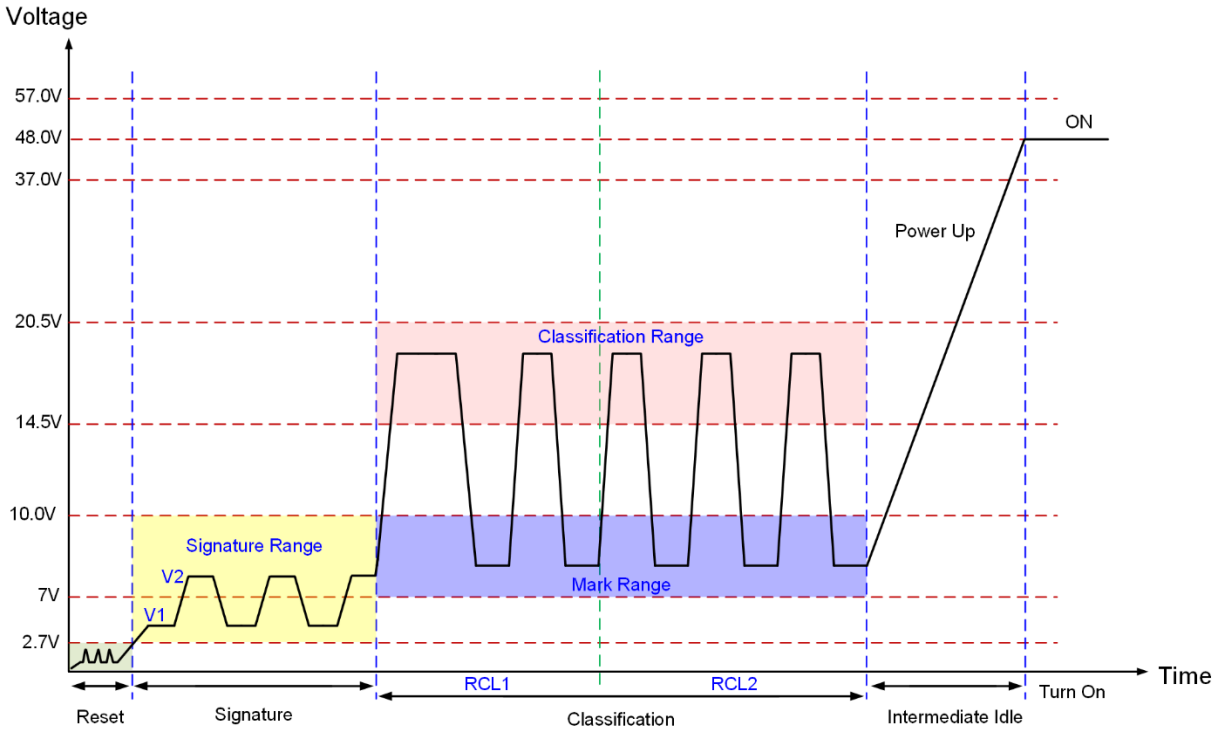


Figure 3. IEEE 802.3bt Typical Power-On Waveform

PoE BT Power-On Start Up Waveform

1. Voltages V1 and V2 with a minimum 1V difference are applied by the PSE to extract a signature value.
2. The PSE takes current/impedance readings during Class/Mark Events to determine the class of the PD. At this time, the PD presents a load current determined by the resistances connected to the RCLASS pins (RCL1 and RCL2)
3. After the PSE measures the PD load current, a high-power PSE will present a mark voltage (6.9-10V), followed by a classification voltage (14.5V-20.5V). The PD responds by presenting a load current as determined by RCL1 and RCL2. After the PSE measures the PD load current during several class events and determines that it can deliver the requested power, the PSE steps up to an on state to provide full 48V PoE BT Power.

PST1, PST2 and PSDBT Pins

PST1, PST2 and PSDBT are Open Drain active-low output pins that indicate PSE type and power level to a system controller. PSDBT output pin provides an indicator when a Type 3 or 4 PSE (bt PSE) is detected. PST1 and PST2 output pins indicate the allocated power level. The PSDBT, PST1, PST2 pins will be set low once the PD recognizes the related conditions and completion of the internal power good (PG) signal is set high after V_{OD} power up. These output pins will remain low and will only be reset high by the occurrence of a Reset or a power-down event.

The state of PST1, PST2 and PSDBT is used to provide information relative to the PSE Type (1-2 or 3-4) and its allocated power. Table 4 lists the encoding corresponding to various combinations of PSE Type, PD Class and allocated power. Since PST1, PST2 and PSDBT signals are open-drain active low outputs, each pin should be terminated to VDD5 using 10kΩ resistor.

Demotion conditions also correspond to cases where the PSE allocated power is lower than what the PD is requesting. The allocated power is determined by the number of classification cycles received by the PD. KTA1142 power demotion details and PST1, PST2 and PSDBT status are provided in Table 5.

Table 4. KTA1142 Power LEVEL Details based on PST1, PST2 and PSDBT Pins Status

PSE Type	PD Class	# Class Events	PSE Allocated Power LEVEL	PST1	PST2	PSDBT
1 or 2	0	1	12.95	High	High	High
1 or 2	1	1	3.84	High	High	High
1 or 2	2	1	6.49	High	High	High
1 or 2	3	1	12.95	High	High	High
2	4	2	25.5	Low	High	High
3 or 4	0	1	12.95	High	High	Low
3 or 4	1	1	3.84	High	High	Low
3 or 4	2	1	6.49	High	High	Low
3 or 4	3	1	12.95	High	High	Low
3 or 4	4	2 or 3	25.5	Low	High	Low
3 or 4	5	4	38.25	High	Low	Low
3 or 4	6	4	51	High	Low	Low
4	7	5	62	Low	Low	Low
4	8	5	71.3	Low	Low	Low

Table 5. KTA1142 Power Demotion Details

PSE Type	PD Class	# Class Events	PSE Power LEVEL	PST1	PST2	PSDBT
3 or 4	4-8	1	12.95	High	High	Low
3 or 4	5-8	2,3	25.5	Low	High	Low
3 or 4	7-8	4	51	High	Low	Low

Local Power Mode (LVMODE)

The LVMODE pin can be used in applications where the PD appliance is designed to draw power from either the Ethernet cable or an external DC local power adapter. LVMODE pin is a voltage mode input pin with low and high thresholds as defined in the electrical characteristics for the PD. LVMODE is asserted when the input exceeds the input high threshold at 1.7V and is de-asserted when the input voltage is less than the threshold 1.2V VLVMODE threshold. If LVMODE operation is not desired, the LVMODE pin should be terminated to AGND.

Referring to Figure 4, a simplified internal circuit diagram and external application circuit are required to use the LVMODE feature. When power is applied at the local adapter input, the KTA1142 enters Local Voltage Mode. This opens the internal Hot-Swap FET switch while the internal DC-DC controller is in operation. The local power input has priority over PoE power input, irrespective of their relative voltage levels. If local power is removed, the device will exit Local Voltage Mode operation and revert to PoE power if available.

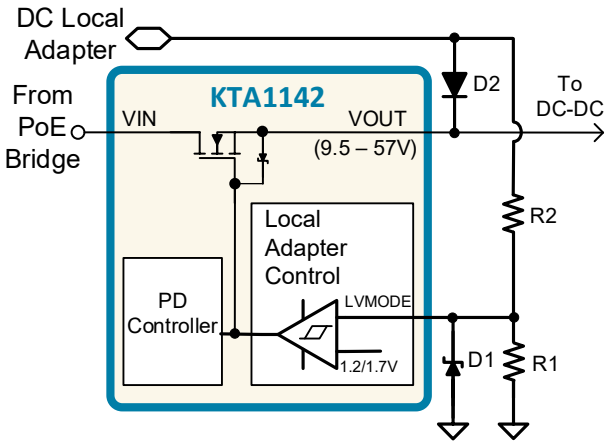


Figure 4. LVMODE Implementation

Connecting a resistive divider between the LV/MODE pin and the Local Power Input engages the local power input start-up voltage with hysteresis. Refer to Figure 4 for the recommended circuit connection. To achieve a target 40V turn on point (V_{Local_On}) for typical a 48V Local Power application, select R1 first. 30.1KΩ is a recommended starting point for R1. R2 can then be calculated by following $\boldsymbol{R2} = (\boldsymbol{V_{Local_{On}}} - \mathbf{1.7}) * \boldsymbol{R1} / \mathbf{1.7}$ Equation **2**. For example, if 30.1kΩ is used for R1, the resulting R2 value would be 680kΩ.

$$\boldsymbol{R2} = \frac{(\boldsymbol{V_{Local_{On}}} - \mathbf{1.7}) * \boldsymbol{R1}}{\mathbf{1.7}} \qquad \text{Equation 2.}$$

Local power is inserted at the VOUT node (VOD pin) through an external diode (D2). The D2 can be replaced by the KTS1900 ideal diode controller and Power FET for high efficiency applications. When using an external diode for D2, use of a low reverse-leakage diode is recommended. This ensures that when there is no local power, PoE voltage at the VOUT node will not falsely pull up the LVMODE pin due to high reverse leakage through the diode.

An appropriate ratio of R1 and R2 resistors should be used to ensure current circuit operation across all supply voltage levels. Though common values of R1 and R2 can be used across the whole range of local supply voltages from 9.5V to 57V, using higher value pairs will minimize power consumption. The maximum input voltage at the LVMODE pin should not exceed 6V. A Zener diode (D1) is recommended to limit transient voltage excursion on this input. In addition to configuring the device for operation from a local power source, the external power transformer must also be designed to ensure proper operation across the local power input range.

Since the input voltage at the LVMODE pin defines its state, it is not recommended to drive other circuits or components directly from the LVMODE node (such as an indicator LED) that might draw excess current causing LVMODE input voltage errors. Indicator LEDs or current-absorbing components should be driven directly from the Local Supply input.

Table 6. LVMODE Configuration

Local Voltage Range	Recommended Local Adapters
9.5V-57V	12V, 18V
20V-57V	24V, 30V
32.4V-57V	36V, 48V

PD Controller Power and Thermal Protection

The KTA1142 provides the following PD controller power and thermal protection:

- Internal default Under Voltage Lock Out (UVLO) for hot swap FET
- EN/UVLO for external configurations for the hot swap FET
- Inrush Current Limit with integrated current sense
- Thermal Limit / Protection

Under Voltage Lock Out (UVLO) and external EN/UVLO configuration

The KTA1142 contains an internal VIN Under-Voltage Lock Out (UVLO) circuit to determine when the input supply is valid and may power on the PD. The internal PD circuit controls power flow to the downstream DC-DC converter, the UVLO feature is intended to protect the system from erratic or low input supply operation.

The internal UVLO power on rising voltage threshold level is 38V with a power off shutdown threshold at 32V. Additionally, the EN/UVLO input requires a 1.2V or greater signal level is applied for the device to start up. When a valid supply is applied to VIN along with an enable voltage of 1.2V or greater is present on the EN/UVLO pin, the PD will turn on the internal hot-swap power MOSFET switch and the PoE voltage regulator will start up.

For most application circuits, a voltage divider may be placed between VIN and ground to source a VIN in supply driven enable signal for EN/UVLO. It is recommended to use a megaohm resistance range to reduce power dissipation in the resistor divider as the expected VIN supply is in the range of 38V to 57V. Refer to Equation 3 to calculate the required enable resistor divider resistance values.

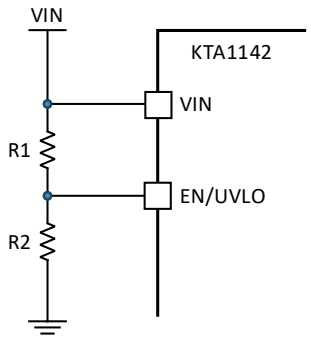


Figure 5. EN/UVLO Resistor Divider Configuration

$$VUVLO = VIN\ x\ \left(\frac{R2}{R1+R2}\right)$$ Equation 3

For a typical application with a standard 48V PSE driven input supply, R1 = 3.9MΩ and R2 = 150kΩ. This will create a nominal 1.8V enable voltage level to be applied to EN/UVLO. This resistor value set will hold EN/UVLO above 1.2V even if the VIN input supply falls to the UVLO shutdown threshold at 32V.

The EN/UVLO enable feature can be driven by an external signal source if required by the system design to have an external enable/disable control. With a valid PoE input supply applied to VIN, the KTA1142 PD will power up and turn on the hot swap switch when the signal to EN/UVLO rises to 1.2V or greater. The EN/UVLO is a logic level input. An externally applied signal should not exceed 6V per the absolute maximum voltage rating for this input.

If EN/UVLO is not used, it should be terminated to VDD5. The KTA1142 PD UVLO function will follow the internal default UVLO to power on threshold at 38v and power off at 32V.

Inrush Current Limit / Current Sense

Inrush limiting maintains the cable voltage above the 32V UVLO turn-off threshold as the input capacitor charges. This also prevents the PSE from going into current limiting. The Current Limit/Current Sense circuitry minimizes PD on-chip temperature peaks by limiting both inrush and operating current.

During the PD startup sequence, current through the internal Hot-Swap FET is momentarily high as the VOUT output capacitance is charged up. During this state, the Hot-Swap FET experiences a high instantaneous power dissipation from the I^2R drop which results in device heating. It is recommended that during this startup sequence, the incoming current should only be utilized for the charging of the VOUT node, to minimize the startup time and associated power drop across the FET. There is a total 108ms time for inrush. PD over current protection (OCP) will be active after the inrush timing is complete. The PD OCP function has a debounce time of 512µs.

Thermal Limit / Protection

The KTA1142 provides on die thermal protection. The internal die temperature is monitored and will reduce the maximum current through the device or disconnect power as needed to prevent the die temperature from exceeding the preset thermal limit at 160˚C. If adverse operating conditions cause the internal die temperature to exceed 160°C, the device will shut down. Normal operation will resume when the die temperature drops below 125˚C.

Maintain Power Signature and AMPS

The IEEE 802.3bt standard requires the load on a PSE to be greater than 20mW or it must shut down to conserve power. To keep a PSE active during light-load or no-load conditions, the KTA1142 provides a “Maintain Power Signature” or MPS feature to comply with the BT standard. The MPS current level is user set for a 10mA, 16mA or 20mA current pulse. Refer to table 8 for the MPS current set resistor value. For PSE type 1 and 2 operating conditions, the MPS current pulse and duty cycle are fixed 88ms/224ms on and off timing. Under PSE type 3 and 4 operating conditions, the MPS duty cycle is user programmable. Refer to table 7 for MPS duty cycle timing and programming. If the MPS feature is not needed, it may be disabled by leaving the AMPS pin unconnected (open).

Table 7 shows the details for MPSD pin termination to select the MPS duty cycle for a given PSE type operation.

Table 7. Maintain Power Signature Duty Cycle Selection Details

PSE Type	MPSD Pin Resistance Value	Duty Cycle	Ton	Toff
1, 2	-	-	88ms	224ms
3, 4	GND	12.5%	20ms	140ms
3, 4	60.4kΩ	8.1%	16ms	184ms
3, 4	Open	5.4%	12ms	210ms

Automatic Maintain Power Signature (AMPS) control can be assigned by AMPS pin with a resistor and appropriate power rating to support the MPS current.

Table 8. Maintain Power Signature Current Amplitude Selection Details

Conditions	AMPS Pin Resistance Value	MPS current Amplitude
1	237kΩ	10mA
2	150kΩ	16mA
3	118kΩ	20mA

Auto-Class

Auto-Class is a classification mechanism that allows a PD to communicate its effective maximum power consumption to the PSE. This happens in such a way that the PSE will be able to set the power budget to the effective maximum for the PD power. This feature was introduced by the IEEE802.3bt standard to allow for a more efficient use of the available power. The KTA1142 PD supports Type 3 or Type 4 PD Auto-Class whereas a Type 3 or Type 4 PSE has the option to make use of it to optimize its power management.

A PSE implementing Auto-Class uses the first-class event to inquire if the PD supports Auto-Class, looking for the class current to fall to a class 0 current level. If the condition is met, the PSE can then proceed to Auto-Class measurement immediately after power up. The PD is then required to draw its highest power throughout the bounded period using a sliding time window to calculate the power.

To enable the KTA1142 Auto-Class feature, the AUT pin should be terminated to AGND. If the Auto-Class feature is not used, it may be disable by leaving the AUT pin unconnected (open).

DC-DC Controller Details

The KTA1142 has a peak current mode active clamp PWM controller that integrates all the circuitry required to design a smart and efficient converter for PoE and telecom mid-power DCDC converter applications. KTA1142 features a programmable oscillator for the switching frequency, adjustable slope compensation, dual low-side MOSFET gate drivers with programmable dead time, soft-start, frequency dithering, maximum duty limit, and a self-start internal high-voltage linear regulator.

The controller is mainly intended to be used for active clamp forward/flyback converter topologies for small and mid-power PoE regulator applications up to 72W.

The controller provides two MOSFET gate drive outputs, the main power switch control (G1) and the active clamp switch control (G2). The main output driver, G1, is designed for driving a forward/flyback converter primary MOSFET. The secondary output, G2, is designed for driving an active clamp circuit MOSFET, or a synchronous rectifier on the secondary side of an isolated supply.

Startup Sequences

When EN/UVLO pin is not used, the internal PoE UVLO (Undervoltage Lock Out) circuit holds the Hot-Swap switch off before the PSE provides full voltage to the PD. This prevents the downstream converter circuits from loading the PoE input during detection and classification.

The PSE drives the primary voltage to the operating range once it has decided to power up the PD. When Vin rises above the UVLO turn-on threshold (approximately 38V), KTA1142 enables the Hot-Swap MOSFET with inrush current limit.

During the input current inrush period, the DC/DC Controller is turned off providing a no-load supply voltage to the PWM controller to avoid additional loading that could prevent a successful PD event and subsequent converter start up. After the initial current inrush is finished (typically around 10ms, depending on the actual inrush current and VOD capacitor value), the VOD voltage is charged to VIN. The DC/DC Controller starts up and the downstream DC-DC converter starts loading from VOD. This always occurs 100ms after the inrush current start point. The PD OCP function is valid at this event.

MOSFET Gate Drive Outputs G1 / G2

The G1 and G2 integrated MOSFET drivers can supply up to 1.5A peak source and sink current. G1 is intended for driving the main primary side switching MOSFET, while G2 is used for an auxiliary function, depending on the voltage regulation circuit topology selected. For typical applications, G2 will control a P-channel auxiliary MOSFET referred to PGND in active clamp forward topologies. The dead time is controlled by the resistor value from DT pin connected to AGND pin of the controller. The rising edge dead time and the falling edge dead time are identical. DT can be adjusted to fine tune the relative switching times of the MOSFETs to maximize the converter efficiency.

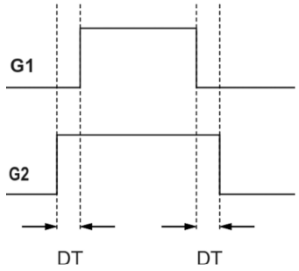


Figure 6. Time Relation between Output Drivers and DT

Gate Driver Dead Time (DT) Function

The relative phase of the main switch gate driver G1 and active clamp gate driver G2 can be configured for multiple applications. Active clamp configurations utilize a ground referenced P-Channel clamp switch, the two gate driver outputs should be in phase with the active clamp output overlapping the main output. Switch dead time is controlled by a resistor connected between the DT pin to AGND. The rising edge dead time and the falling edge dead time are equal. To set or adjust the switching dead time, refer to the curve of Dead Time vs. Programming Resistance in the typical Characteristics section of this data sheet. The suggested DT resistance should range from 10kΩ to 200kΩ. Please refer to $\boldsymbol{T_{DT}}\mathbf{ns} = \mathbf{2.4} * \boldsymbol{R_{DT}}(\mathbf{K\Omega})$ Equation **4** below to calculate programmed dead time vs R_{DT} resistor value.

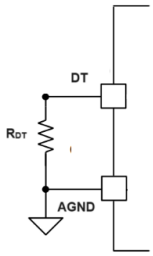


Figure 7. Dead time configuration

$$T_{DT}(\mathbf{ns}) = 2.4 * R_{DT}(\mathrm{K\Omega}) \quad \text{Equation 4}$$

A default dead time of 60ns is set by leaving the DT pin unconnected (floating). For user set dead time programming, the R_{DT} resistor should be connected as closely to the DT pin as possible. For Flyback circuit topologies the DT feature is not needed because a FET active clamp is not used, the G2 gate driver signal may be left un-terminated.

Converter Switching Frequency

The KTA1142 internal oscillator frequency is user set by the external resistance connected between the FREQ pin and AGND. The switching frequency may be user configured over a 75kHz to 1MHz frequency range to meet system requirements depending upon specific regulator topologies being employed. The R_{FREQ} resistor value may be determined by using Equation 5 below. The resulting resistance value may be rounded to the closest 1% resistor value for a given switching frequency. For programing switching frequency details, please refer to the Switching Frequency vs. Programming Resistance curve in the typical Characteristics section for this datasheet. For default fixed switching frequency operation, the frequency dithering feature is not used. The DITHER/SYNC pin should be terminated to AGND pin with a 10nF capacitor or connected to a 3.3V or 5V high logic voltage.

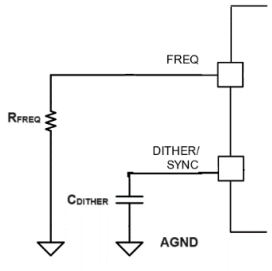


Figure 8. Frequency configuration

$$R_{freq} = \frac{1}{F_{freq} * 4.2 * 10\hat{}-11} \quad \text{Equation 5}$$

Frequency Dithering and Synchronization Features (DITHER/SYNC)

The KTA1142 has a internal clock frequency dithering or synchronization function to aid in application circuit EMI reduction. When the DITHER/SYNC pin is configured for Frequency Dithering, the switching frequency of the converter will be dithered by an amount set by an external C_{DITHER} capacitor. The DITHER/SYNC input also allows the KTA1142 switching frequency oscillator to be synchronized to an external clock source. This can be helpful when multiple PoE regulators are used in the same system or to force a specific switching frequency to mitigate EMI or RF interference.

For normal frequency dithering operation, a ceramic capacitor is placed between the DITHER/SYNC pin and AGND. An internal current source at the DITHER/SYNC pin charges the capacitor C_{DITHER} to 2V with a 50µA (I_{DITHER}) current. Upon reaching this 2V trip point, C_{DITHER} will be discharged to 0.4V with a 50µA discharge current. The charging and discharging of the capacitor generates a triangular waveform on DITHER/SYNC with bottom and peak levels of 0.4V to 2V.

The resistor (R_{DITHER}) connected from DITHER/SYNC to FREQ determines the amount of frequency dither from the base switching frequency set by the R_{FREQ} connected to the FREQ pin and AGND. The approximate dither frequency range can be calculated using Equation 6 below. Refer Equation 7 for the triangular waveform frequency (modulation frequency).

For example, when setting R_{DITHER} to 5 times R_{FREQ}, it will generate and approximate ±13.3% dithering of preset regulator oscillator frequency. A C_{DITHER} capacitor value of 10nF will generate a 1.56kHz modulation frequency.

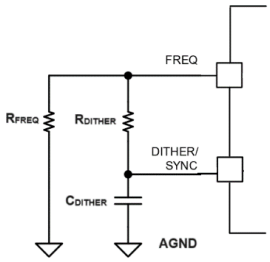


Figure 9. Frequency Dithering Configuration

$$Freq_{DITHER\ Range}(+/-\%) = \frac{2}{3} * \frac{R_{FREQ}}{R_{DITHER}} * 100\% \qquad \text{Equation 6}$$

$$Freq_{Modulation} = \frac{1}{2} * \frac{I_{DITHER}}{C_{DITHER} * 1.6} \qquad \text{Equation 7}$$

The KTA1142 has a default dithering frequency capability that can be enabled by connecting DITHER/SYNC directly to AGND. Default frequency dithering is fixed at ±7% of the preset regulator oscillator frequency as set by the R_{FREQ} resistor connected from the FREQ pin to AGND. The default modulation frequency is 1/64 of FREQ pin settled oscillator frequency. This feature is useful to provide a minimum level of frequency dithering to reduce EMI effects of the PoE regulator circuit while saving PCB space and external component cost by eliminating the need to use the dither programming resistor and capacitor.

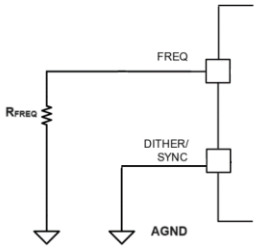


Figure 10. Frequency Dithering Default Configuration

The KTA1142 regulator switching frequency synchronization feature is enabled by connecting an external-clock signal directly to the DITHER/SYNC pin. The internal oscillator frequency will be synchronized to the applied input signal. The external synchronizing clock signal period should be within a 110% to 130% range of the free-running internal oscillator frequency set by the FREQ pin resistor. The acceptable minimum pulse-width of the synchronization signal must have an on-time 400ns or greater. The external synchronization signal level should be 0V to 2.9V or greater while not exceeding the maximum voltage rating for the DITHER/SYNC pin.

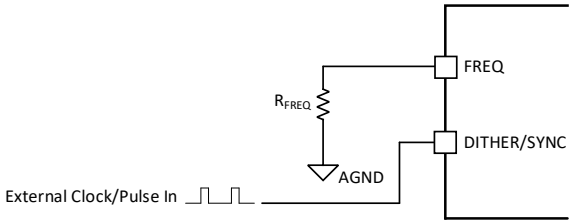


Figure 11. Frequency Dithering / Sync Disable Configuration

If the frequency dithering or sync features are not used, the DITHER/SYNC pin should be terminated to AGND using a 10nF ceramic capacitor to disable the function. Conversely, the 10nF terminating capacitor may be connected to a 3.3V or 5V high logic voltage source to achieve the same result.

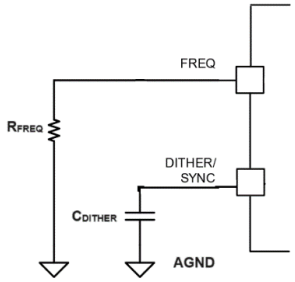


Figure 12. Frequency Dithering / Sync Disable Configuration

Soft Start /Soft Stop

The soft-start time is programmed by a capacitor (C_{SS}) connected between the SS pin to AGND. During startup, this capacitor is charged by a constant 10µA (I_{SS})current, the C_{SS} capacitor voltage rises accordingly. This slowly rising voltage ramp on the SS pin (V_{SS}) limits the COMP voltage during startup. The COMP voltage is clamped at 0.8V higher than SS pin voltage during startup ($V_{COMP} = V_{SS} + 0.8$). This slowly rising and clamped voltage on the COMP will achieve soft start timing for DC-DC converter applications during startup. Soft start begins when V_{SS} is around 0.1V and terminates when VSS reaches an internal voltage at 1.2V. The V_{SS} voltage will continue to rise until it reaches a steady state level equal to VDD5.

For an application with a nominal 100nF C_{SS} capacitor value, the soft start time will be close to 10mS.

Refer to Equation 8 to determine the optimal value for the SS capacitor (C_{SS}) for a given soft startup time (T_{START}).

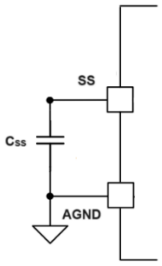


Figure 13. Soft Start and Soft Stop Configuration

$$C_{SS} = \frac{I_{SS} * T_{START}}{V_{SS}}$$ Equation 8

Where:
I_{SS} = 10µA
V_{SS} = 1.2V – 0.1V = 1.1V
T_{START} = Desired Soft Start Time for the System
C_{SS} = Soft Start Capacitor Value

To prevent oscillations in self-driven synchronous rectifiers on the secondary side of the converter during turnoff, the KTA1142 has a soft stop feature. When a fault OCP, OTP, or turn off event occurs, the SS pin voltage falls slowly from 5V by a constant 10µA discharge current. When the SS voltage drops below 1V, the COMP pin voltage will be clamped 0.8V higher than SS pin voltage when turning off which lets the COMP voltage slowly drop and the DC-DC converter can then achieve a soft stop. The soft stop finishes when SS pin voltage (V_{SS}) drops to approximately 0.2V where the controller will fully turn off. The soft stop time is similar to the soft startup time if ignoring this 0.2V.

Current Mode Feedback and Current Sense Input

The CS pin input provides a control ramp for the pulse width modulator and current limit detection for overload protection.

The DC-DC controller of KTA1142 is a peak current mode active clamp controller. The current through the external Main MOSFET is measured through a current-sense resistor that is connected in series between the MOSFET's source and ground. The sensed voltage on the CS pin is then amplified and fed to the PWM comparator for current mode control. The current comparator takes this amplified current sensed voltage (plus slope compensation) as one of its inputs, then compares this value with the VCOMP-0.8V. When the voltage exceeds VCOMP-0.8V, the comparator outputs low, and the power MOSFET turns off.

If the sensed voltage at CS exceeds 0.3V and remains at that level for approximately 32 cycles, the over-current protection will trigger and enter soft stop. A small RC filter, located near the controller, is recommended for the CS input pin. A 65ns blanking time is applied at the start of each main switch cycle to attenuate any leading-edge spikes on the current sense signal. After soft stop, the controller will restart after a fixed delay time. The delay time is defined as 34000 times of the oscillator switching cycle set by the FREQ pin resistor.

To avoid reaching current limit threshold (V_{CSD}), the designed voltage (V_{CS}) across the current-sense resistor (R_{CS}) should be less than the current limit voltage. In order to avoid unwanted mis-triggering of the current limit protection, the designed V_{CS} should be set to 70% of V_{CSD} at the rated output load. Typically, 70% of V_{CSD} can be adjusted based on real system requirements, the range should be 60% to 80% of V_{CSD} in most cases. The R_{CS} resistor value can be estimated by Equation 9.

$$R_{CS} = \frac{70\% * V_{CSD}}{I_{PEAK}}$$ Equation 9

Where:

I_{PEAK} is the primary-side peak current

V_{CSD} is the current limit threshold

70% is the typical value to design V_{CS} to avoid reaching to V_{CSD} under normal condition

Example: A typical forward regulator application may have V_{IN} = 48, V_{OUT} = 12V, I_{OUT_MAX} = 6A, F_{sw}= 250K, with the following transformer turns ratio N_P:N_S = 1.6:1, L_M = 70µH, L_O = 6.1µH.

The I_{PEAK} is 6.33A, the R_{CS} is calculated =$\frac{70\%*300mV}{6.33A}$=33mΩ

For this example, a current sense resistor with a standard value that is as close as possible to 33mΩ should be selected.

A small RC filter, located near the controller, is recommended for the CS input pin. Typically, R = 100Ω and C = 1nF will achieve a 100nS time constant providing a good anti-ringing filter for the current sense signal.

PWM Comparator and Slope Compensation

To control isolated flyback/forward voltage-regulator topologies, the error amplifier is located externally from the KTA1142 (usually implemented with a Texas Instruments TL431 Adjustable precision shunt regulator), and the feedback signal is taken from the collector of a feedback optocoupler. Current is sensed through a current-sense resistor (RCS) connected between the source of the primary-side main switching MOSFET and PGND.

The sensed voltage on the CS pin is internally amplified by 4× and fed to the PWM comparator for current-mode control. The comparator uses the amplified current-sense voltage (plus slope compensation) as one input and compares it against the voltage on the COMP pin minus 0.8 V (V_{COMP} − 0.8V). The COMP pin is internally pulled up to a fixed 5V reference through an integrated 3.1kΩ resistor, or it can be configured as high impedance, depending on whether FB is tied to VDD5 (3.1kΩ) or GND (high impedance).

Under light-load to no-load conditions, the PWM comparator halts the gate-driver signal (pulse skipping) when the internal PWM-comparator input drops below 200mV. This input consists of the COMP-node voltage minus 800 mV, plus the slope-compensation ramp. PWM skip-mode operation is typically observed when the COMP input voltage is approximately 1V or less.

Under full-load conditions, the internal PWM controller limits the maximum duty cycle to approximately 82%.

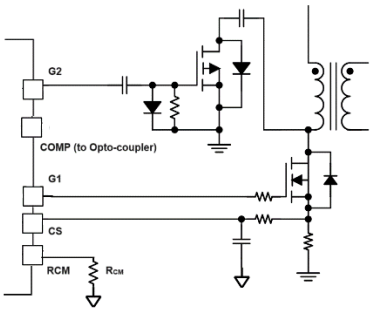


Figure 14. Typical Slope Compensation configuration

The KTA1142 integrates a peak current-mode controller for the PD DC/DC power stage. During CCM (continuous conduction mode) operation—especially when the PWM duty cycle is close to or greater than 50%—current-mode control loops can exhibit subharmonic oscillation without slope compensation. To maintain stable operation under these conditions, slope compensation is required. The KTA1142 provides on-

chip, user-programmable slope compensation to address this issue. Slope compensation is implemented by adding an external resistor (R_{CM}) from the RCM to AGND pin (see **Figure 14**). Slope compensation is not required when the DC/DC power stage operates in DCM (discontinuous conduction mode).

The KTA1142 slope-compensation ramp is fixed by design at 1.8mV/(µs·kΩ) (page 8, S_{AVC}). The required amount of slope compensation is defined by the stability requirements of the inner peak-current loop. When the slope of the applied compensation ramp equals the downslope of the transformer secondary-inductance current waveform (reflected across the primary-side current-sense resistor), this minimum compensation value applied through the R_{CM} pin prevents current-loop instability. The R_{CM} value can be estimated using the following equations, based on the selected transformer turns ratio and inductance parameters.

Slope compensation is needed in the following conditions:

When operating in CCM mode

1. When the PWM switching duty cycle D ≥ 50%

The solution is to add a slope compensation factor $m_{c(falling)}$>1.5

Definitions of constant and variable terms used in slope compensation formulas and equations:

N = transformer turns ratio

N_P = transformer primary turns value

N_S = transformer secondary turns value

L_P = Transformer primary winding inductance (H)

L_S = Transformer secondary winding inductance (H)

V_{OUT} = Regulator Output Voltage (V)

$m_{C(valley)}$ *= Slope compensation (falling)*

S_{NV} = Natural slope of the flyback converter system [V/s]

S_{AVC} = Design parameter, Page 8

R_{CS} = Primary FET current-sense resistor value [Ω]

I_S = current, secondary side

I_P = current, primary side

Transformer Turns Ratio:

$$N = \frac{N_S}{N_P}$$

Transformer Secondary side natural valley current slope:

$$\frac{dI_S}{dt} = \frac{-V_{OUT}}{L_S}$$

Reflected secondary natural valley current slope to the transformer primary side current:

$$\frac{dI_P}{dt} = \frac{V_{OUT}}{N \times L_P}$$

Transformer primary side sensed slope (voltage sensed via the current sense resistor R_{CS} connected between the primary FET switch source and ground):

$$S_{NV} = \frac{V_{OUT}}{N \times L_P} \times R_{CS} \quad [V/s]$$

Recommended slope compensation for a KTA1142 CCM design with D > 0.5:

$$m_{C(valley)} = 1 + \frac{S_{AV}}{S_{NV}} > 1.5$$

$$S_{AV} = \frac{1}{2} \times S_{NV}$$

$$S_{AV} = S_{AVC} \times R_{CM} \, [k\Omega]$$

Slope compensation resistor (R_{CM}) value:

$$R_{CM} = \frac{0.5 \times S_{NV}}{S_{AVC}} \quad [k\Omega]$$

S_{AVC} is referred to the CS (sense) input. Because S_{NV} and S_{AV} are both referred to that same node, the current-sense amplifier gain cancels in the ratio and does not appear in the mc(valley) expression — the characterized coefficient S_{AVC} (1.8 mV/(µs·kΩ)) already accounts for it. Equivalently, $m_{C(valley)}$ = = 1 + (S_{AVC} × R_{CM}) / S_{NV}, and the R_{CM} required for a target $m_{C(valley)}$ is R_{CM} = ($m_{C(valley)}$ − 1) × S_{NV} / S_{AVC}.

Voltage Mode Feedback

The FB pin is the voltage feedback point for the internal error amplifier. The KTA1142 controller is commonly used for isolated regulator application systems (Flyback or Forward) where VOUT is regulated for an isolated secondary side. In these cases, the VOUT signal is fed back to the COMP pin through the optocoupler and the internal error amplifier of KTA1142 is not used. For isolated regulator applications, terminate this pin to VDD5 or GND. For non-isolated regulator applications, connect FB pin to the resistor divider sense network to regulate the output voltage.

Internal Linear Voltage Regulators

VDD5 5V Regulator

The KTA1142 has an integrated linear regulator to power internal control circuitry, the PD controller and to provide a stable supply for logic level interface signals. The VDD5 regulator is powered from the VIN supply pin and provides a typical 4.7V output supply rail. This regulator is active when power is applied to VIN and the device is enabled to support KTA1142 PD functions. For the best voltage regulation performance, the VDD5 pin should be bypassed with a 1.0µF or greater value ceramic capacitor. The VDD5 supply output rail is intended to support KTA1142 logic and control and well as to supply interface logic signals only. It is not intended to power other accessory circuits to minimize device power dissipation from the linear voltage regulator.

VDD10 10V Regulator

The KTA1142 also contains a 10V linear regulator that is powered from the downstream side of the hot-swap MOSFET switch which is also tied to the VOD switched supply. The VDD10 linear regulator provides a 10V output to power the internal gate driver circuits (G1 and G2). For the best voltage regulation performance, the VDD10 pin should be bypassed with a 1.0µF or greater value ceramic capacitor.

To reduce power loss with this internal regulator and prevent excess controller power dissipation, an external regulated voltage supply should be applied to the VOD pin. This external voltage regulator is usually powered from an auxiliary transformer winding. The external regulated voltage at the VOD pin should be greater than

11.5V to shut off the internal start-up regulator and not exceed 15V to prevent going over the maximum ratings for the VDD10 pin.

PCB Layout Guidelines

Thermal De-Rating and Board Layout Considerations

The KTA1142 is capable of operating to an industrial temperature range of 85°C in ambient air and up to 125°C junction temperature, without forced cooling. A thermal pad on the underside of the package dissipates the heat generated by the PD die.

In higher power applications, designers must consider thermal dissipation as an integral part of their system architecture and plan to remove heat via this pad.

For adequate heat dissipation, the board layout must include a ground pad which provides both the ground connection and dissipates the heat energy produced in the chip. Thermal vias are used to draw heat away from the PD package and to transfer it to the backside of the system PCB.

Besides the layout for thermal consideration, the following layout guidelines are recommended for optimum system performance.

1. Keep DC-DC converter power stage loops area as small as possible for minimal noise and ringing.
    a. Input power loop: Input capacitors (VOD net), Primary of Transformer, Main MOSFET, Current sense resistor.
    b. Output power loop: Secondary of Transformer, Output capacitors, Rectifier Diodes or MOSFETs.
    c. Active-clamp loop: Input capacitors (VOD net), Primary of Transformer, active-clamp MOSFET and Capacitor.
2. The KTA1142 has an analog/signal ground, AGND, and a power ground, PGND. AGND is used for analog/signal connections such as FREQ, DT and other signal pins. PGND is used for high power connections such as the output drivers, G1 and G2 pins. All the analog/signal ground tracks should be connected in common near the IC AGND, and then a single connection made from the KTA1142 signal ground to the DC-DC converter power ground (sense resistor ground point).
3. The DC-DC converter current-sense circuit normally employs a current sense resistor. The sense resistor is connected between the Source of primary side Main MOSFET and the power ground terminal. A low inductance resistor should be used for this application. The negative terminal of the DC-DC input power capacitor, the ground return of the MOSFET, and current-sensing resistor should be placed as close together as possible. The filter network for the current-sense feedback circuit should be located close to the KTA1142 IC CS pin as possible.
4. The gate drive outputs of the KTA1142 should have short direct paths to the MOSFETs to minimize inductance in the PCB traces, wider PCB traces are recommended for these gate drive loops.
5. Place all components (VDD5 and VDD10 pin capacitor, DT pin resistor, etc.) to their respective grounds and place these components close as possible to the IC to decouple noise. These components and traces should be kept as far away as possible from noise generating nodes (such as the primary Main MOSFET switching node).

Applications Circuits

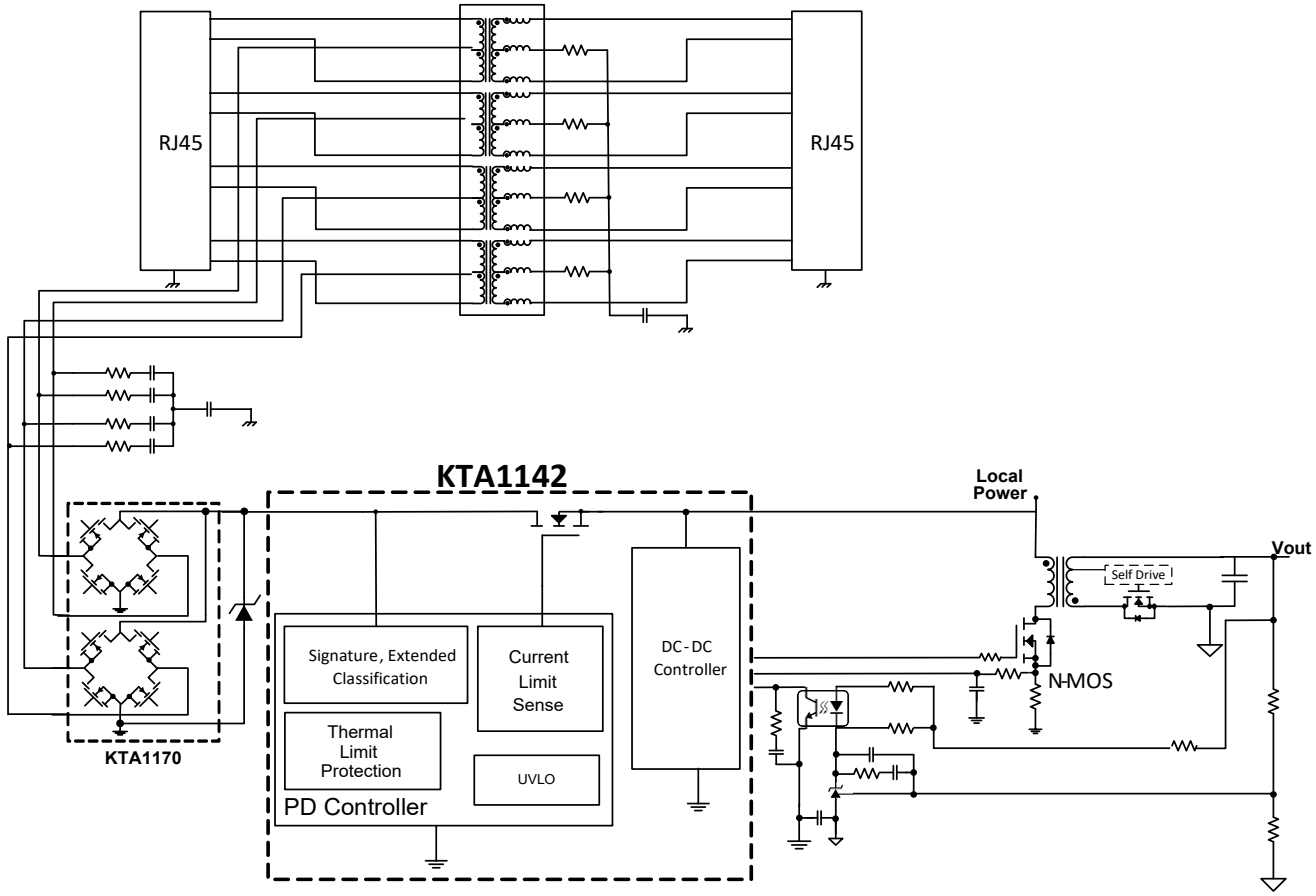


Figure 15. KTA1142 High-Efficiency Flyback DC-DC Solution with Self Drive Synchronization

Note: This is a simplified conceptual schematic. Please refer to reference design documentation for detailed design and component information.

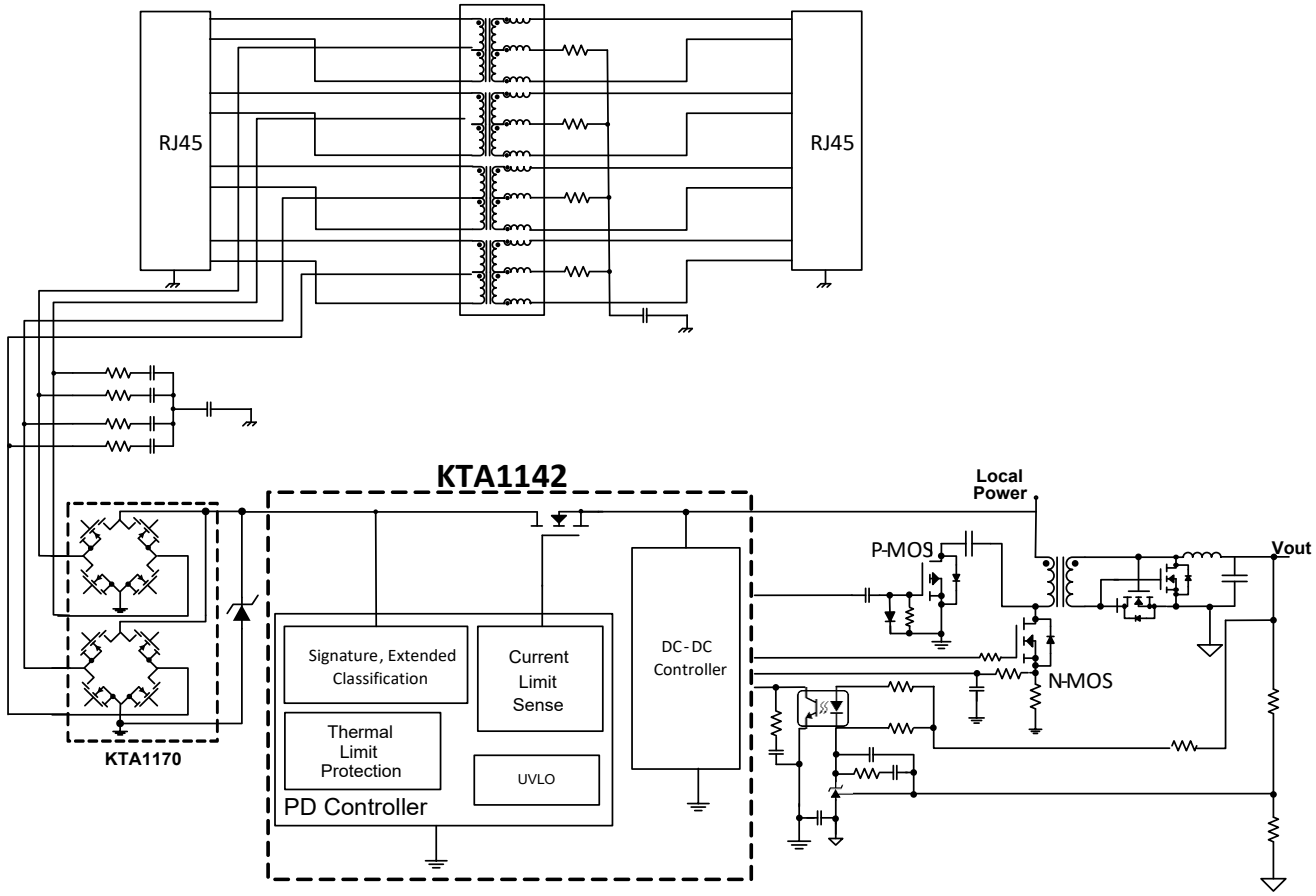
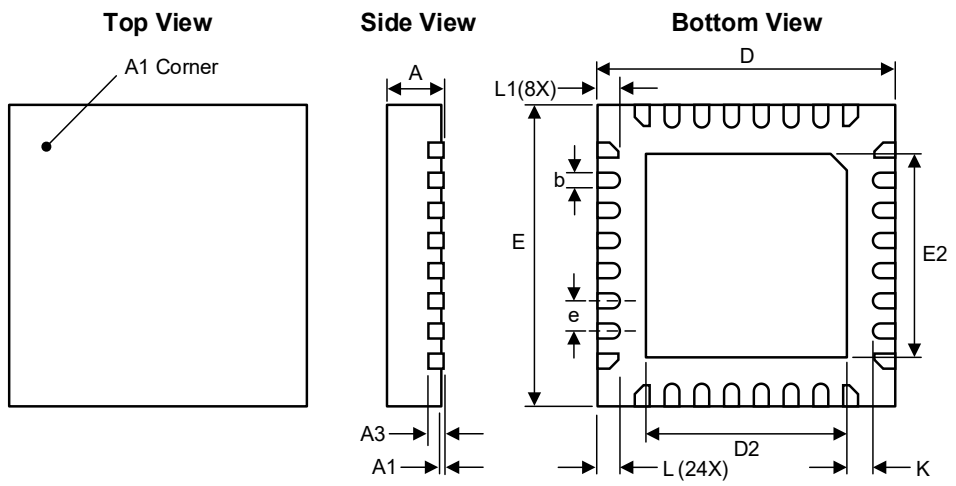


Figure 16. KTA1142 High-Efficiency Active Clamp Forward Solution for Higher Current Applications

Note: This is a simplified conceptual schematic. Please refer to reference design documentation for detailed design and component information.

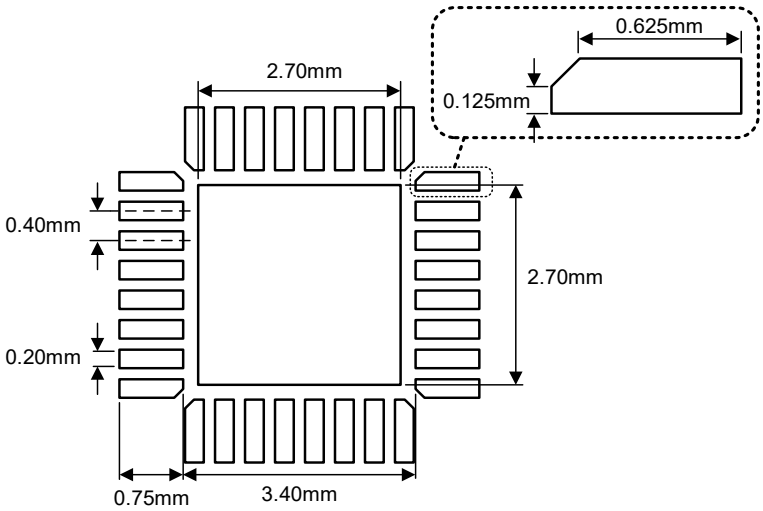
Packaging Information

WQFN44-32 (4.00mm x 4.00mm x 0.75mm)



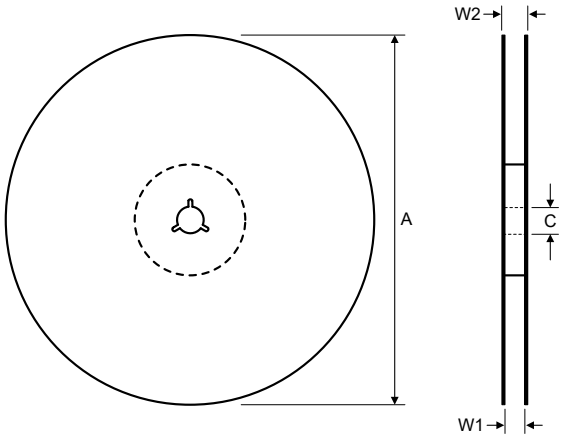
Dimension	mm		
	Min.	Typ.	Max.
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3		0.203 REF	
b	0.15	0.20	0.25
D	3.90	4.00	4.10
D2	2.65	2.70	2.75
E	3.90	4.00	4.10
E2	2.65	2.70	2.75
e		0.40 BSC	
K	0.20	–	–
L	0.25	0.30	0.35
L1	0.23	0.28	0.33

Recommended Footprint



Packing Material Information

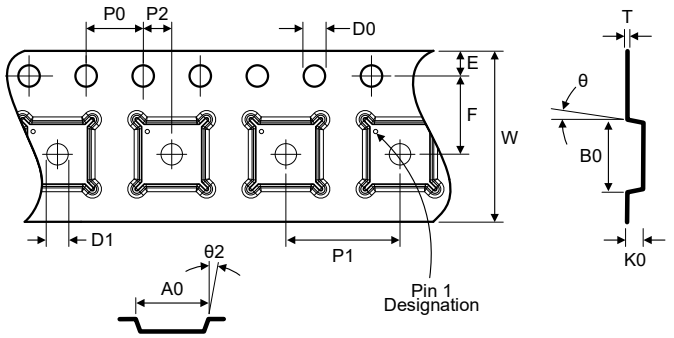
Reel Dimensions



Dimension	mm		
	Min.	Typ.	Max.
A	176	178	180
C	12.8	13.0	13.5
W1	12.4	12.4	14.4
W2	—	—	18.4

DWG-0261-01

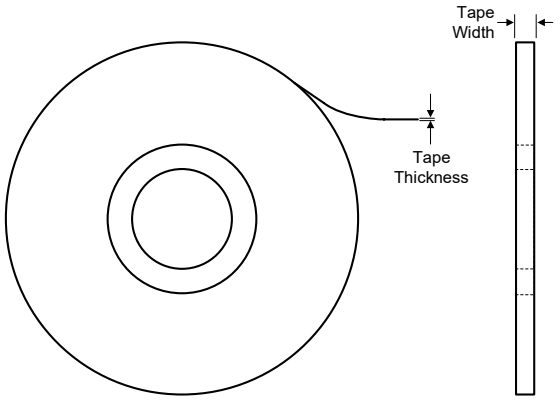
Carrier Tape Dimensions



Dimension	mm		
	Min.	Typ.	Max.
A0	4.20	4.25	4.30
B0	4.20	4.25	4.30
K0	1.00	1.10	1.20
P0	3.80	4.00	4.20
P1	—	8.00	—
P2	1.95	2.00	2.05
D0	1.50	1.50	1.60
D1	1.50	—	—
E	1.65	1.75	1.85
F	5.45	5.50	5.55
10P0	38.0	40.0	42.0
W	11.90	12.00	12.30
T	0.25	0.30	0.35
Θ	0°		5°
Θ2	0°		5°

DWG-0268-01

Cover Tape Dimensions



Dimensions	Dimension	mm		
		Min.	Typ.	Max.
	Tape Thickness	0.040	0.050	0.06
12mm	Tape Width	9.2	—	9.5

DWG-0259-01