

B0549-SCH-01

RD1-4028 VEGA STDP4028 (DVI to DPTx) Reference Design

PCB# 400-533

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## Revision History

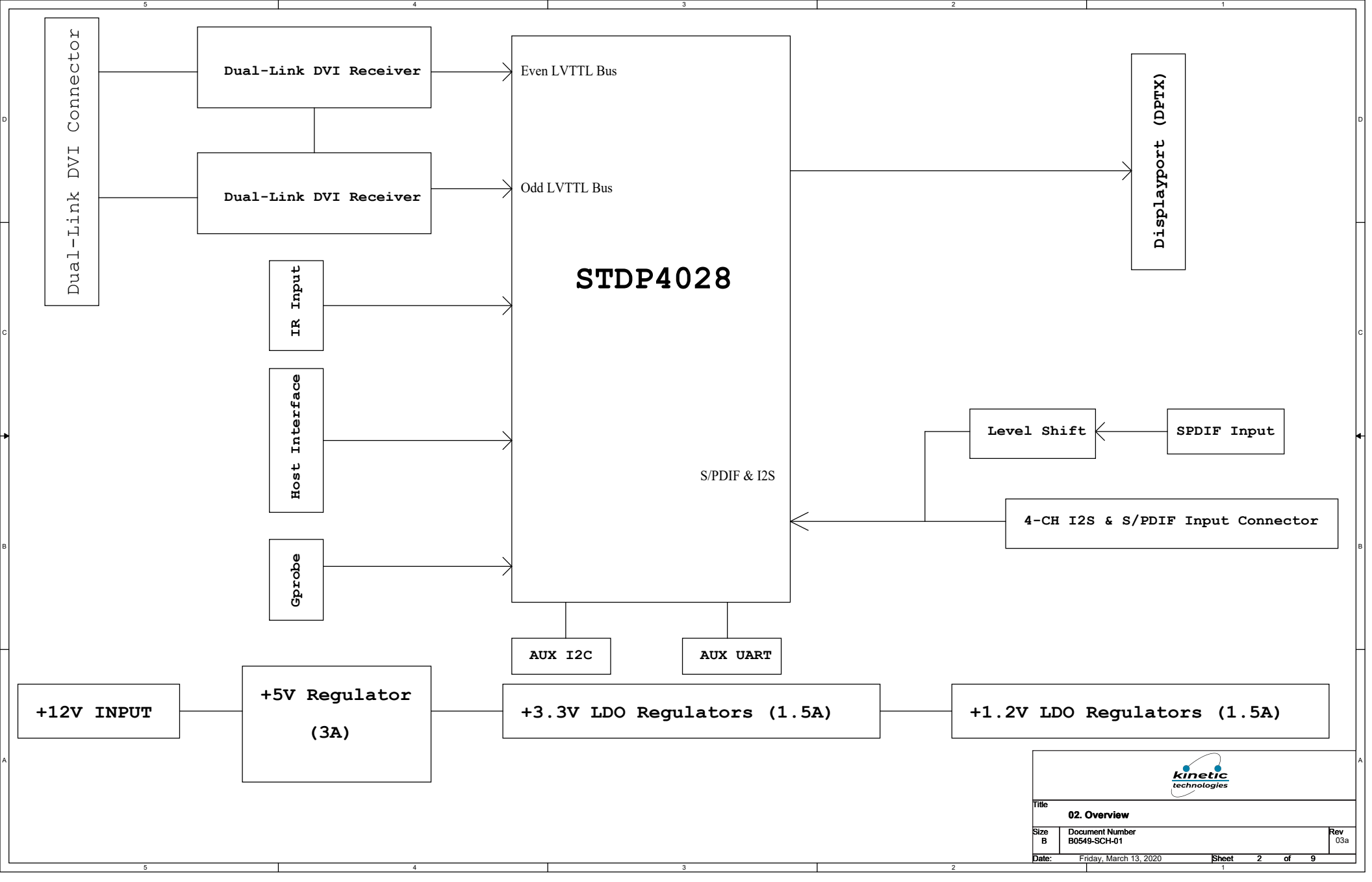
Date	Version	Comments
Sept. 15, 2009	Rev. A	Initial schematic.
Oct. 22, 2009	Rev. A1	Swapped BS2 with BS4
June 8, 2010	Rev. B	Removed U605 (Optional Oscillator) Removed D601 & Q601
July 27, 2010	Rev. C	Updated VEGA STDP4028 TTL Mapping
July 19, 2011	Rev. D	Updated Default BootStrap Settings
Sept 26, 2014	Rev. D	Changed Titleblock and logo to MegaChips
March 11, 2020	Rev. 03a	Update to Kinetic format.

### Layout Notes:

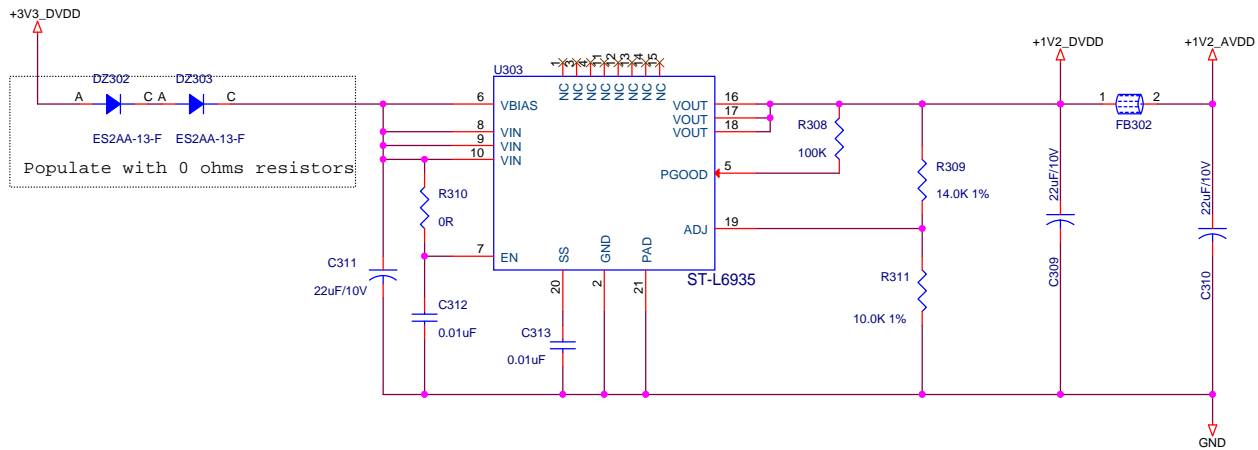
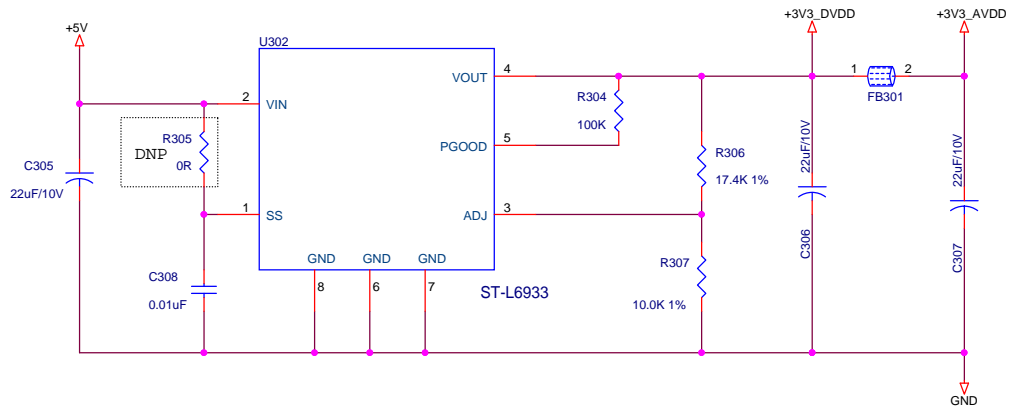
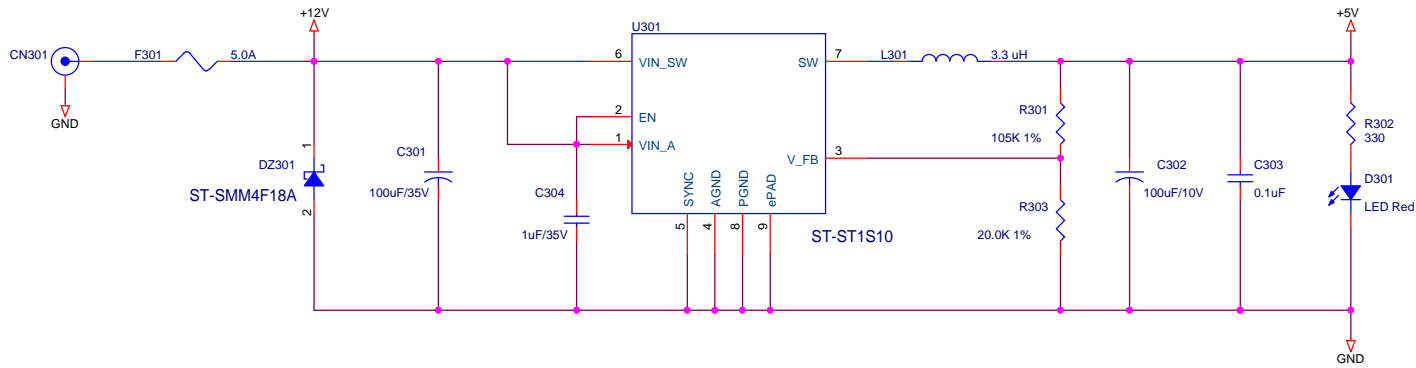
1. 50 ohms impedance on all LVTTTL traces
2. 100 ohms differential impedance on all DP & LVDS trace pairs
2. 4 Layers PCB, \*\*\* Top, GND, PWR, Bottom \*\*\* ,THK = 0.062 inches



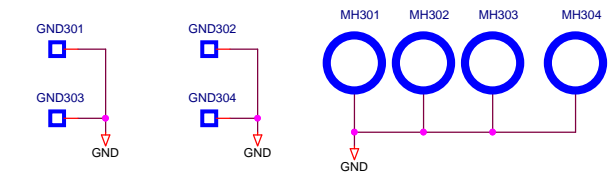
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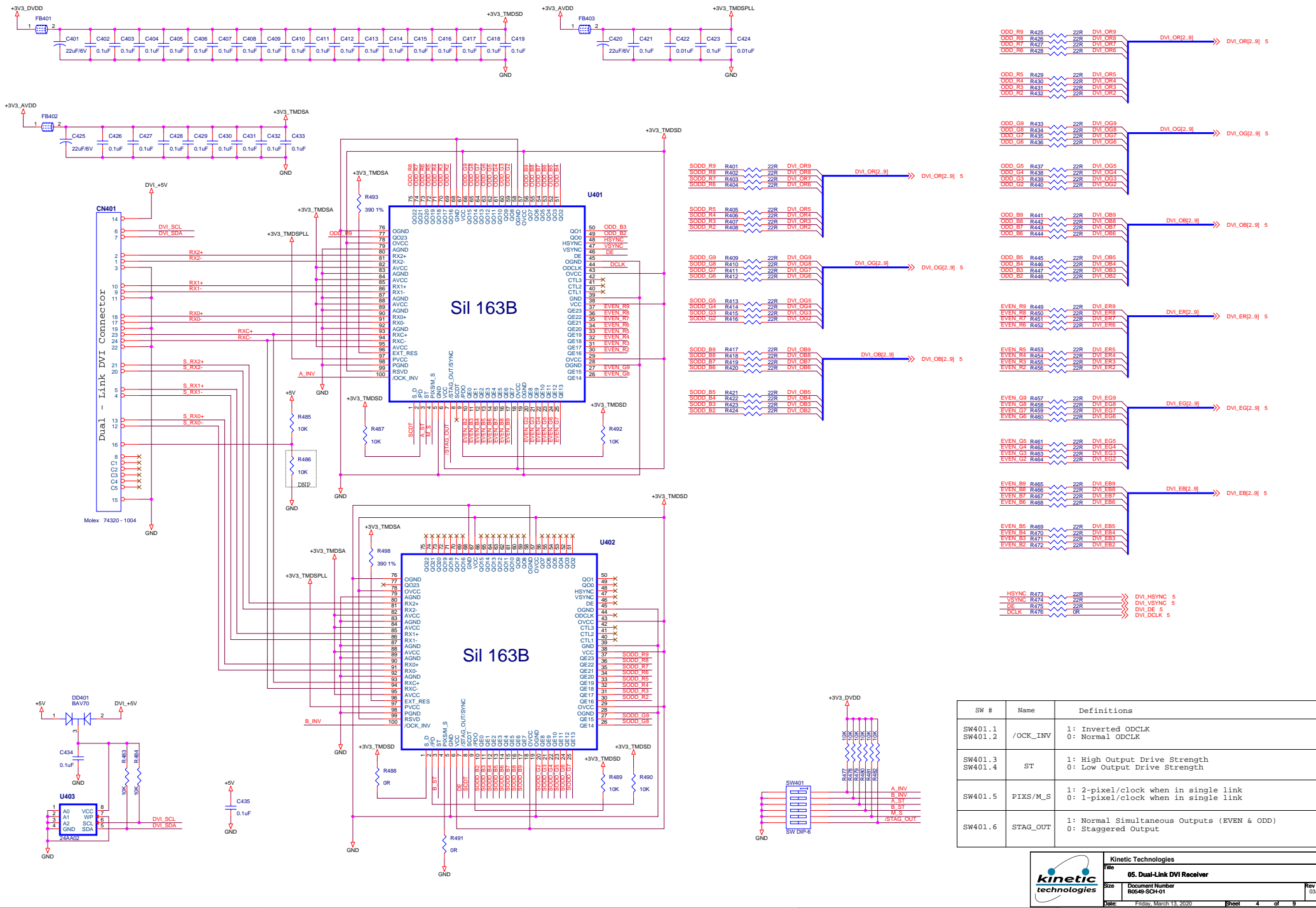


Title		
02. Overview		
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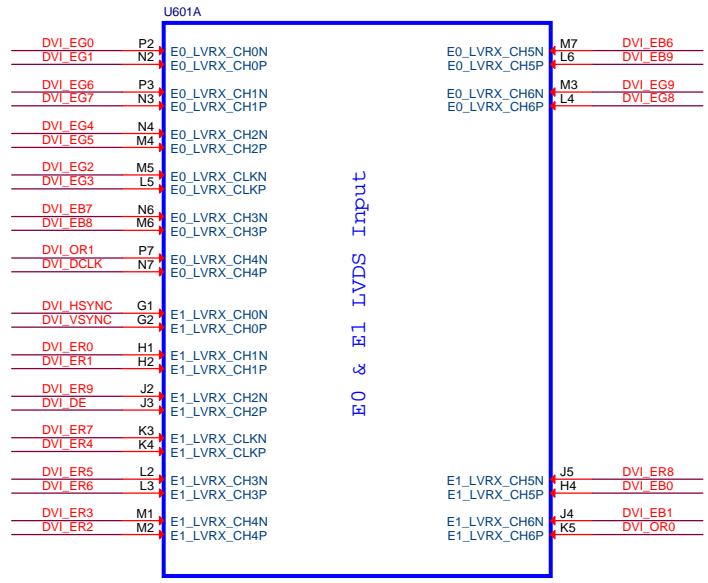


DZ302    DZ303  
 A    C A    C  
 ES2AA-13-F    ES2AA-13-F  
 Populate with 0 ohms resistors

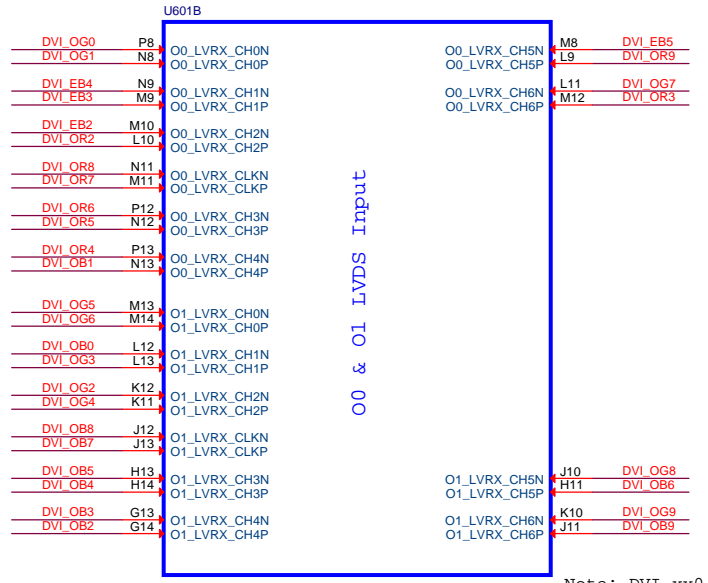




SW #	Name	Definitions
SW401.1	/OCK_INV	1: Inverted OCLK 0: Normal OCLK
SW401.3	ST	1: High Output Drive Strength 0: Low Output Drive Strength
SW401.5	PIXS/M_S	1: 2-pixel/clock when in single link 0: 1-pixel/clock when in single link
SW401.6	STAG_OUT	1: Normal Simultaneous Outputs (EVEN & ODD) 0: Staggered Output

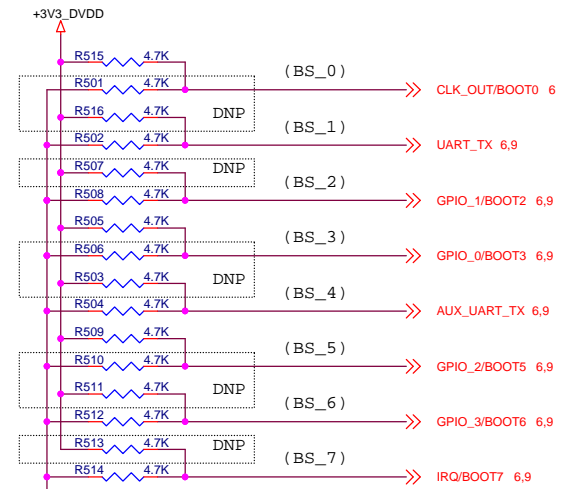
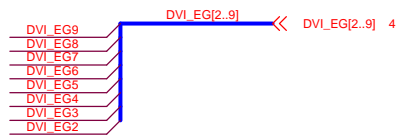
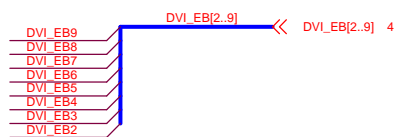
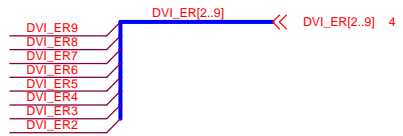
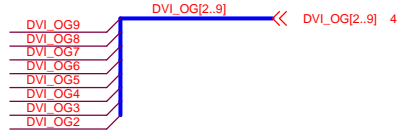


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Note: DVI\_xx0 and DVI\_xx1 are for 10 bits color mapping only

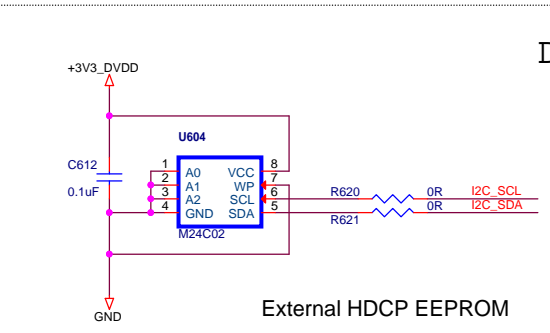
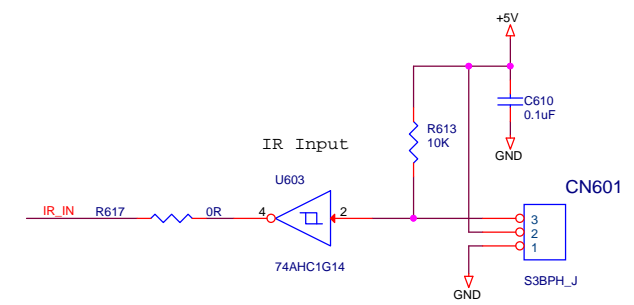
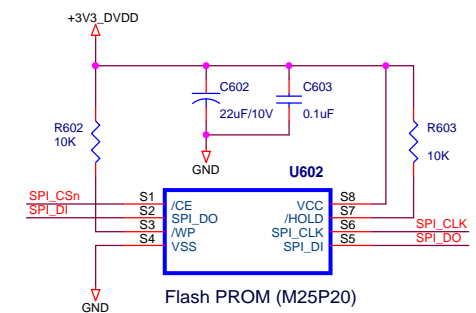
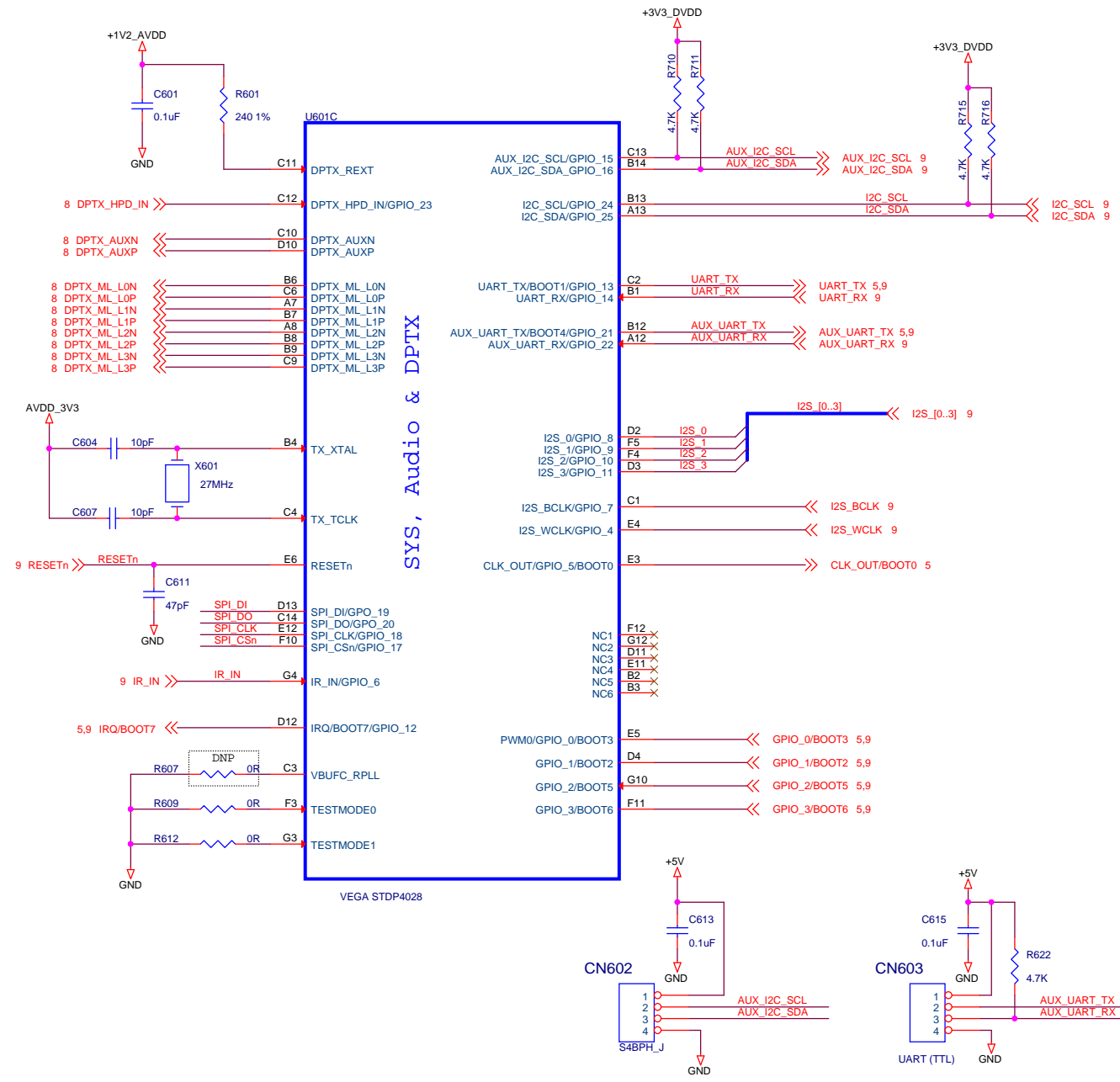


VEGA STDP4028 DPTx BootStraps

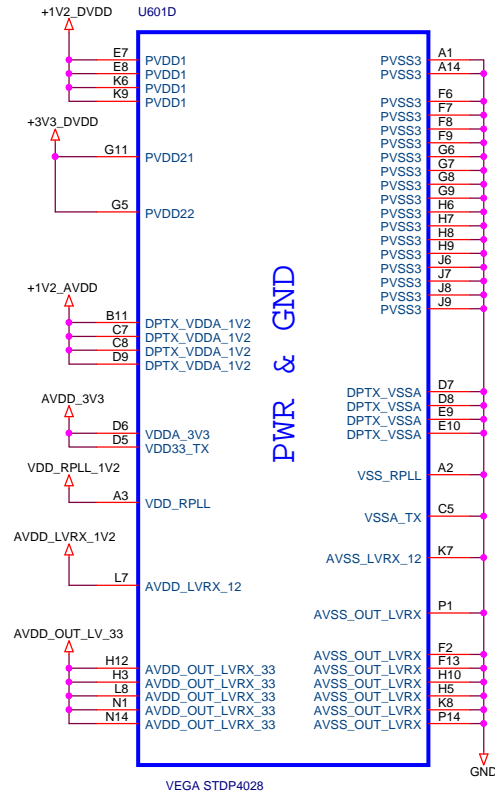
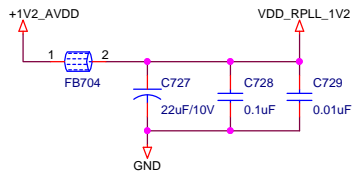
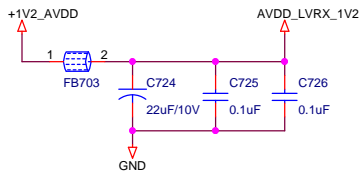
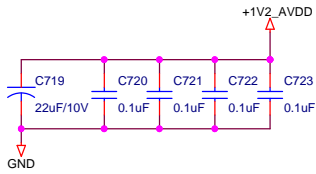
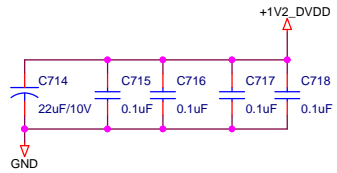
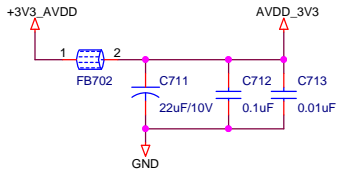
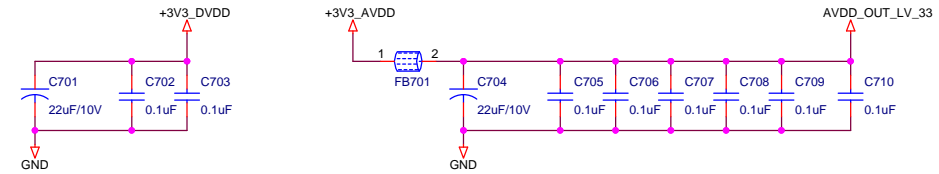


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SYS, Audio & DPTX



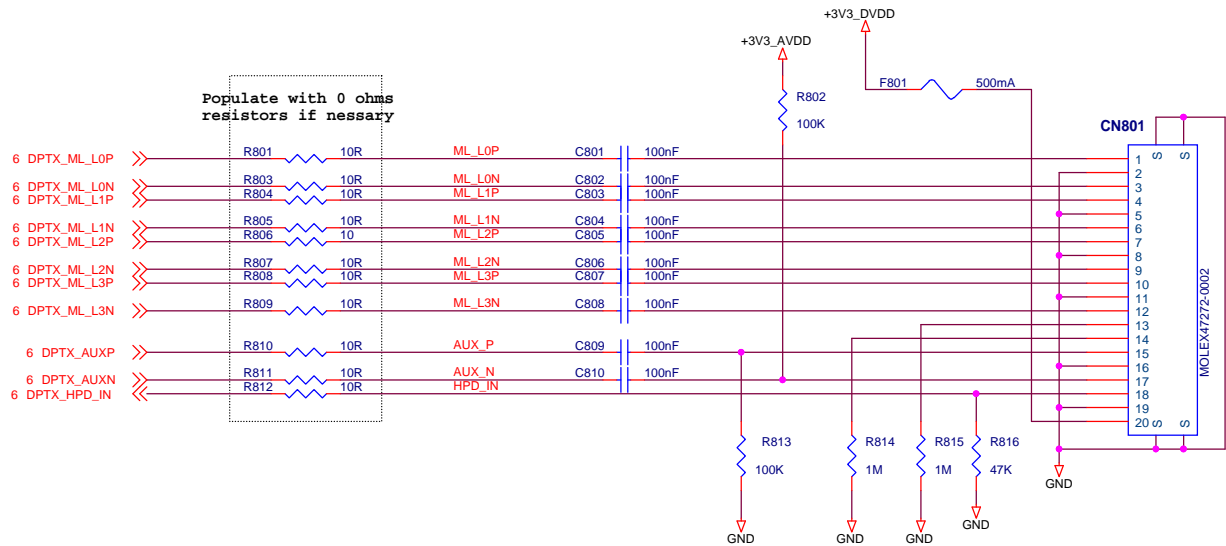
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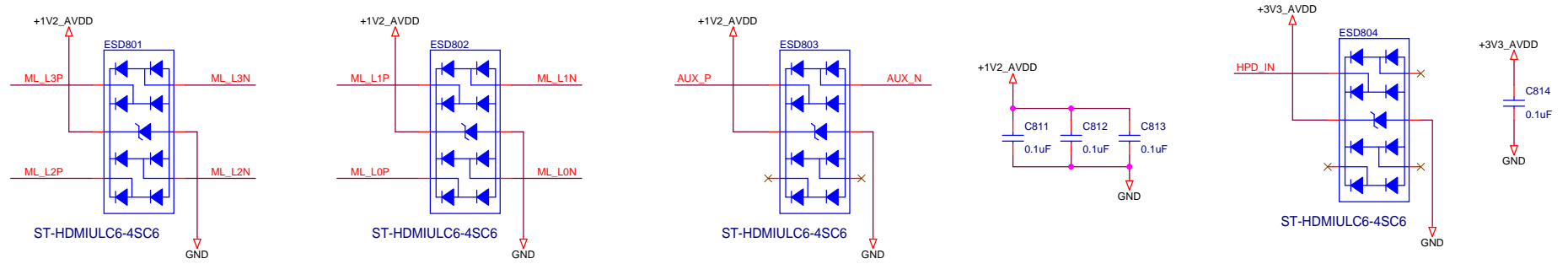
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Title		
08. STDP4028 --- PWR & GND		
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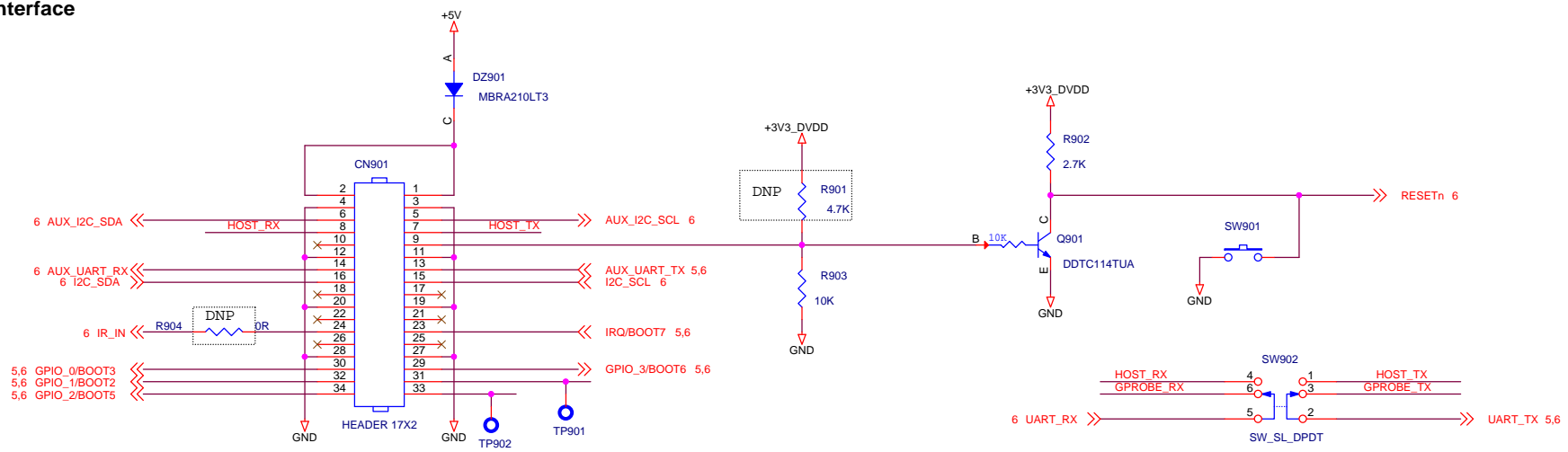


DPTX





# Host Control Interface



# Digital Audio Input

