Datasheet Brief

MCDP6000

USB Type-C DP Alt-Mode Switching Retimer

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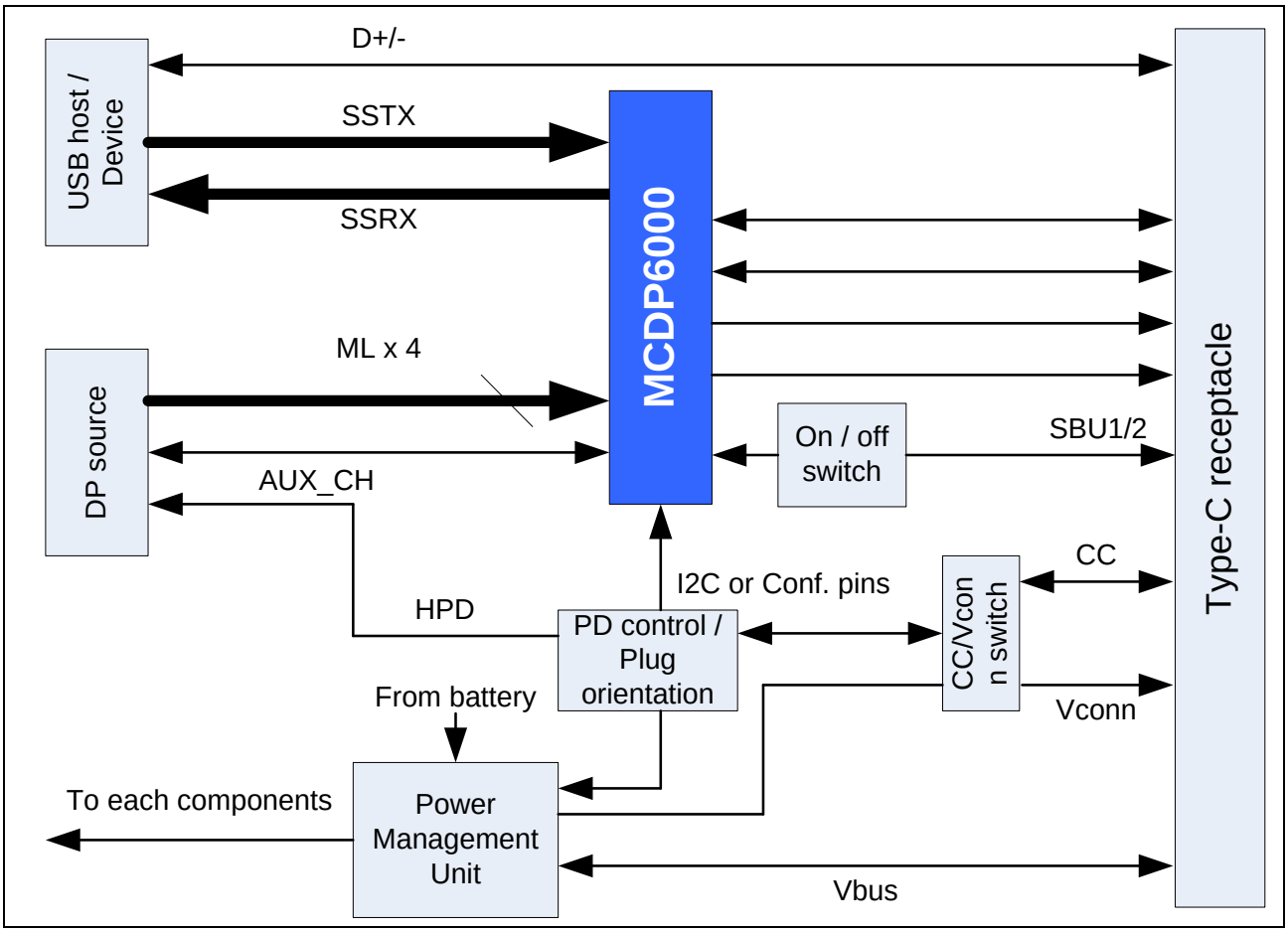
Features

- Integrated USB Type-C DisplayPort alternate mode lane switch to support
  - Flip-ability of USB Type-C
  - Simultaneous USB 3.2 x1 Enhanced SuperSpeed (ESS) and 2 lane DP1.4a
  - 4/2/1-Lane DP1.4a(RBR/HBR/HBR2/HBR3)
- Power Supply Voltages
  - 1.8 V for I/O, 1.2 V for core
- USB3.2 Appendix.E x1 Compliant Retimer
  - 5 Gbps and 10 Gbps support
  - Link training participation
  - Spread-spectrum clocking as per USB 3.2 standard
  - LFPS polling and processing
  - LFPS Based PWM support
  - Pass-Through / Local loopback
  - Loopback BERT for USB 3.2 SS
  - Lane polarity inversion
  - BLR (Bit-Level Retimer) for SS mode
    - Low latency data path
    - Link layer snooping
      - Link power management support
  - SRIS (Separate Reference clock Independent SSC) for SSP mode
    - 128b/132b coding
    - Scrambler / De-scrambler
    - Link power management support
    - SKP OS handling / Elastic buffer for USB for clock offset compensation
    - DC balance tracking / control
    - Error correction
  - Transmitter Emphasis
    - 3-tap FIR TXEQ for SSP
    - 2-tap TXEQ for SS
  - Adaptive Receiver Equalization
    - DFE + CTLE for SSP to support -23dB insertion loss compensation @5GHz
    - CTLE for SS to support -20dB insertion loss compensation @2.5GHz
  - Support of custom PHY configuration through TWI (Two Wire Interface)
- DP1.4a Compliant Repeater
  - Data rate 1.62 Gbps / 2.7 Gbps / 5.4 Gbps / 8.1 Gbps
  - Transparent mode / Non-transparent mode support
  - AUX_CH transaction snooping
  - DP1.4a Compliant Retimer DPCD registers
  - 8b/10b coding
  - Pattern generator and Error Checker
  - Down-spreading of link clock
  - Error detection
  - Adjustable TXEQ during the link training through AUX_CH
  - Adaptive equalizer with CTLE and DFE
    - DFE + CTLE for HBR3 to compensate -27dB insertion loss @4.05GHz
    - CTLE for HBR2 / HBR / RBR
  - Support of custom PHY configuration through TWI
- Real time Eye Opening Monitor (EOM)
- TWI slave to configure the integrated lane mapping and operation mode
  - Compatible with I^2C master
  - Support up to 4 unique TWI device ID
- Configuration pins for the integrated lane switch and operation mode
- Low Power Operation
  - 520 mW in USB 3.2 x1 SSP + Two lanes of DisplayPort HBR3 operation with 1.2 V and 1.8 V power supply
  - 850 µW in standby mode
- ESD Specification
  - 2kV HBM, ±500V CDM
- Package
  - 46 Ex-VQFN (6.5 mm x 4.5 mm)

Applications

- Desktop PC / Notebook / Tablet / Smartphone motherboard enabling USB Type-C DP alternate mode

Figure 1. MCDP6000 System Block Diagram



1. Description

The MCDP6000 is a low power USB 3.2 x1 and DisplayPort1.4a repeater device with an integrated USB Type-C switch targeted for desktop / mobile PC motherboard-down application.

The USB 3.2 x1 retimer supports both SuperSpeed (SS) bit rate (5 Gbps), and SuperSpeedPlus (SSP) data rate (10 Gbps). The USB 3.2 x1 retimer includes the link layer function and LTSSM and RTSSM to participate in the link training. The MCDP6000 supports SS mode with a BLR (Bit-Level Retimer) and SSP mode with a SRIS (Separate Reference clock Independent SSC). The MCDP6000 supports link power management with Ux entry and exits in both SS and SSP modes. In addition, the MCDP6000 supports the link state and link quality maintenance, compensates the clock offset between the downstream port and the upstream port, detects errors, and corrects single symbol errors in framing order sets, single bit block header errors, and single or double-bit SKP symbol errors in SSP mode. It also supports spread spectrum clocking (SSC) to minimize EMI and the low frequency periodic signaling (LFPS). The transmitter employs 3-tap FIR-based transmitter equalizer for SSP operation and fixed transmitter equalizer ranging from 3 dB to 4 dB for SS operation. The receiver employs an adaptive Continuous Time Linear Equalizer (CTLE) and a Decision Feedback Equalizer (DFE). Both the transmitter equalizer and the receiver equalizer are configurable through the TWI register. Proper settings to comply with USB 3.2 electrical requirements are provided by default.

The DP1.4a repeater supports 1.62 Gbps, 2.7 Gbps, 5.4 Gbps, and 8.1 Gbps data rates. The following use cases are supported.

Table 1. DP1.4a Repeater Mode

	Mode	AUX_CH Function
LT tunable PHY Repeater	Non-transparent mode	Sample, Manipulate, and Forward to snoop or respond as defined in DP1.4a standard.
	Transparent mode	Sample and Forward to snoop

The DP1.4a repeater implements AUX_CH snooping function of DPCD addresses defined in the standard as well as the LT-tunable PHY Repeater DPCD registers. The DP1.4a repeater can support up to a 0.5% down-spread link rate. The transmitter employs TXEQ, which adjusts its pre-emphasis level according to either the AUX_CH transaction during the link training or the TWI. The receiver employs a fully adaptive Continuous Time Linear Equalizer (CTLE) and Decision Feedback Equalizer (DFE). The transmitter parameter can be set to support the amplitude level and the pre-emphasis level defined in DP1.4a standard are provided in default.

The MCDP6000 operating mode can be configured through the TWI by default. It can be optionally configured through the 3 configuration pins by enabling the feature through TWI. These interfaces can be controlled from an external Power Delivery (PD) controller or microcontroller to set the plug orientation and the pin mapping of the USB Type-C DP Alt-mode. The MCDP6000 operates at 1.8 V and 1.2 V.

The power consumption is:

1. 520 mW with an active 4 lane retimer (USB 3.2 x1 SSP TX/RX and DP 2 lanes HBR3)
2. 850 µW in stand-by state

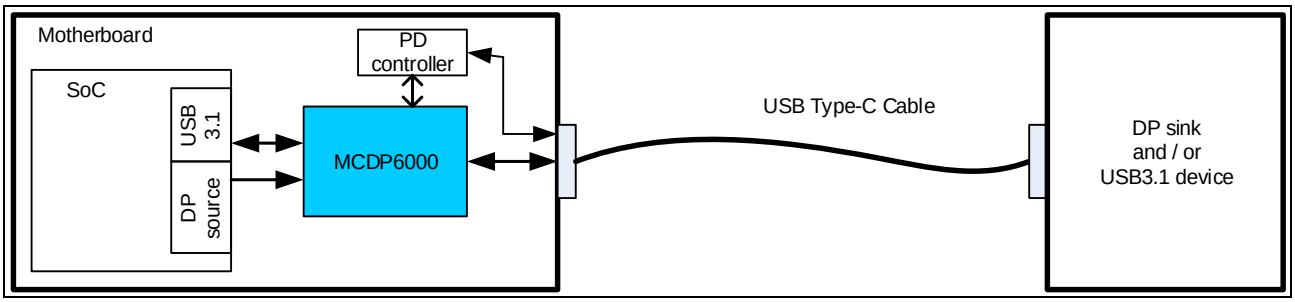
The MCDP6000 is offered in a 46-pin, 6.5 mm x 4.5 mm Ex-VQFN package.

2. Application Overview

The target application of MCDP6000 is the Desktop PC / Notebook / Tablet / Smartphone motherboard enabling USB Type-C DP alternate mode.

The MCDP6000 resides next to the DisplayPort source (CPU/GPU) device, the USB 3.x host or dual-role device, and the Power Delivery (PD) controller on a same PCB with copper tracks connecting directly to these devices. High speed serial interface tracks are typical microstrip lines with controlled impedance of 100 ohm. The MCDP6000 communicates with these devices through either TWI, 3 configuration pins or AUX_CH. By default, the operating mode and the plug orientation are controlled by the PD controller or the Embedded Controller (EC) through the TWI. When the DisplayPort link is discovered by the PD controller, the link training is initiated by the DP source through the AUX_CH.

Figure 2. MCDP6000 Motherboard-Down Use Case



3. Ordering Information

Part Number	Operating Temperature	Package
MCDP6000C1	0°C to +70°C	Ex-VQFN46