Overvoltage Protector with Bidirectional Blocking and Surge Protection

Features

- Wide Input voltage range: 3.0V to +28V
- Integrated MOSFET switch 25mΩ typical
- 5A Continuous Current
- VP Select pin: over-Voltage threshold trip 13V/23.4V
- Fixed 5V Output from VSNS
- Fast Over-Voltage response time 100ns
- Low Quiescent Current: 160µA (typ.)
- Integrated Protection
  - Thermal Shutdown
  - Under voltage protection (UVLO)
  - Soft-Start
  - OUT to IN Reverse Blocking
- $\overline{EN}$, VSNS, $\overline{WRX}$ and $\overline{FLAG}$ pins
- Integrated Surge Protection up to +/-100V
- Pb-free WLCSP 20-Bump, 0.4mm pitch
- -40°C to +85°C Temperature Range

Applications

- Smartphones and Tablets
- Mobile Internet Devices
- Peripherals

Brief Description

The KTS1675A over-voltage protection device features high current integrated N-Channel MOSFETs with an ultra-low IN to OUT on-resistance of 25mΩ (typical). Low-voltage systems on the output are protected from voltage supply faults up to +28V. An internal clamp on the input protects the device from surges up to ±100V.

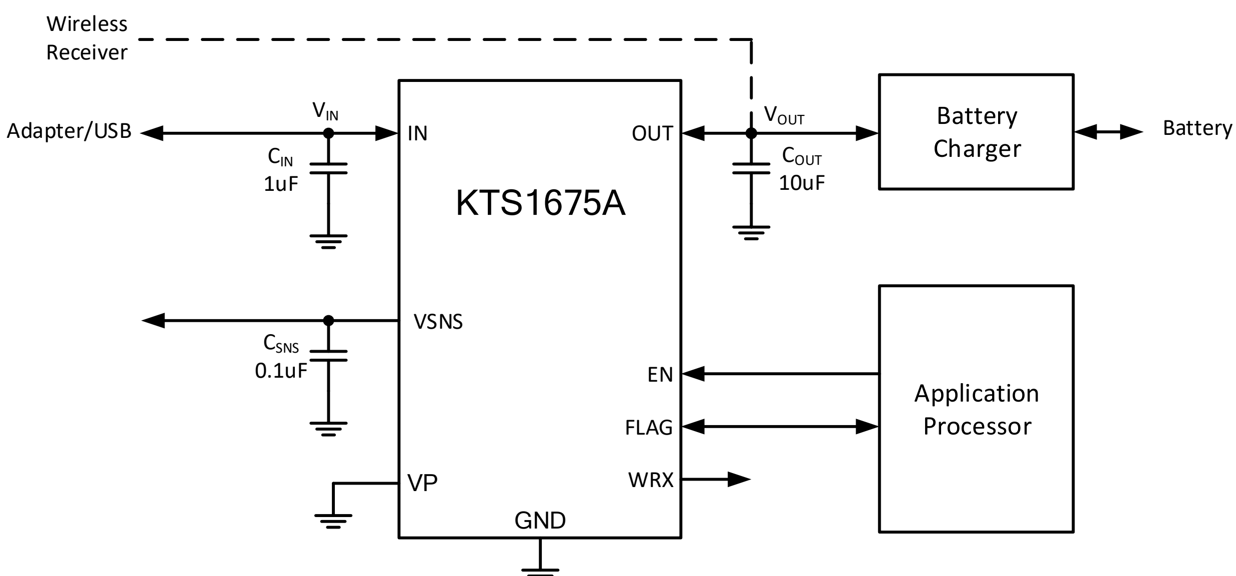
An input voltage exceeding the over-voltage threshold causes the internal MOSFETs to turn off, preventing excessive voltage from damaging downstream devices.

The KTS1675A has a selectable internal fixed OVLO threshold preset to either 13V or 23.4V (typical) and also supports reverse bias blocking, preventing any voltage present at OUT pin feeding back into IN when the device is in the Off state.

The KTS1675A also features additional protection including enhanced ESD and thermal to protect against over-load conditions.

The device is available in a RoHS and Green compliant 20-bump, 0.4mm pitch, 2.22mm x 1.82mm WLCSP.

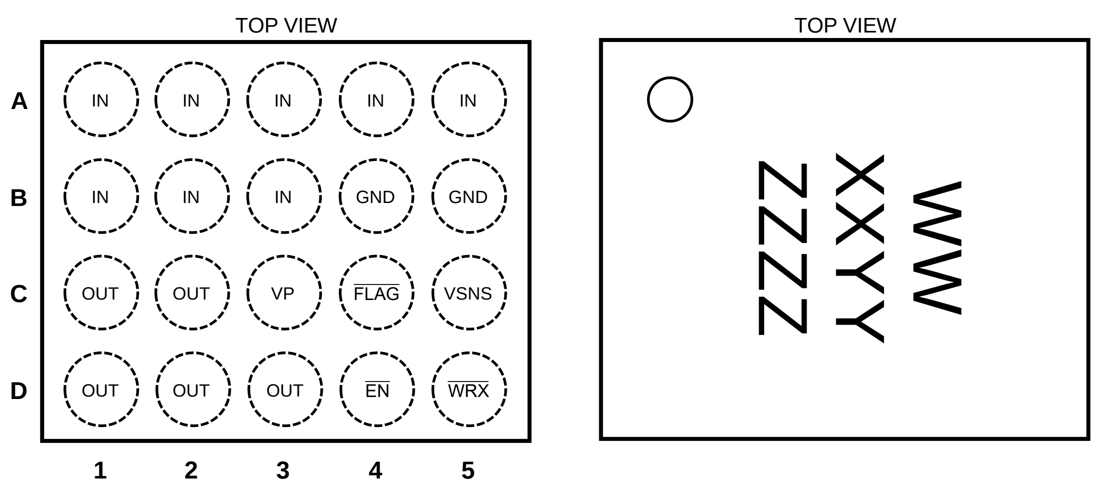
Typical Application



Pin Descriptions

Pin #	Name	Pin Type	Function
A1, A2, A3, A4, A5, B1, B2, B3	IN	Power	Load switch input pin.
C1, C2, D1, D2, D3	OUT	Power	Load switch output pin.
D5	$\overline{\text{WRX}}$	Digital I/O	Wireless receiver (WRx) active low logic enable pin. Slave mode: Pull this pin logic low or Pull this pin to GND. Autonomous mode: Connect this pin to WRx active low enable pin, if a system output control pin is not available.
D4	$\overline{\text{EN}}$	Digital Input	Active low logic enable pin. When $\overline{\text{EN}}$ high, the switch is turned off. Slave mode: Connect this pin to System enable logic pin or tie to external GND plane. Autonomous: Pull this pin logic low or tie to external GND.
B4, B5	GND	Power	Ground pin.
C4	$\overline{\text{FLAG}}$	Digital I/O	$\overline{\text{FLAG}}$ pin is pulled high to indicate to the system when OTG mode can be triggered in autonomous mode. Slave mode: Pull this pin logic low, or tie to external GND. Autonomous mode: Connect to the System digital I/O pin (or equivalent) that pulls logic low to enter OTG mode when IN is connected to an OTG load and a power source is applied to OUT.
C5	VSNS	Analog Output	IN’s voltage indicator. An Internal LDO regulate IN to 5V and output through this pin.
C3	VP	Digital Input	OVP selector pin. Connect VP to GND for a typical 23.4V OVP level. Leave VP floating for a typical 13V OVP level.

WLCSP-20



WLCSP Package 20-Bump 2.22mm x 1.82mm x 0.62mm

Top Mark
WW = Device ID Code,
XX = Date Code, YY = Assembly Code,
ZZZZ = Serial Number

Absolute Maximum Ratings[1]

(T_A = 25°C unless otherwise noted)

Symbol	Description	Value	Units
IN	Input Voltage	-0.3 to 28	V
OUT	Output Voltage	-0.3 to 28	V
IN-OUT	IN to OUT Voltage (when OFF)	-28 to 28	V
$\overline{EN}$, $\overline{FLAG}$, $\overline{WRX}$, VSNS	$\overline{EN}$, $\overline{FLAG}$, and $\overline{WRX}$ and VSNS pins	-0.3 to 6	V
IN, OUT Current	Continuous Current	5	A
T_J	Operating Junction Temperature Range	-40 to 150	°C
T_S	Storage Temperature Range	-65 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

Thermal Capabilities

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance – Junction to Ambient[2]	65	°C/W
P_D	Maximum Power Dissipation at $T_A \leq 25°C$	1919	mW
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-15.4	mW/°C

Ordering Information

Part Number	Marking	Operating Temperature	Package
KTS1675AEUT-TR	NUXXYYZZZZ[3]	-40°C to +85°C	WLCSP-20

Recommended Operating Condition[4]

Description	Value
IN Voltage Range	3.0V to 24V
OUT Voltage Range	3.0V to 24V
Ambient Temperature	-40°C to +85°C
Input capacitance (C_{IN})	Up to 10µF
OTG hot swap capacitance (C_{OTG})	Up to 200µF
Output capacitance (C_{OUT})	Up to 20µF
VSNS capacitance (C_{VSNS})	Up to 1µF

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to a 4-layer board.
3. XX = Date Code, YY = Assembly Code, ZZZZ = Serial Number.
4. The device is not guaranteed to function outside of recommended operating condition.

Electrical Characteristics[5]

V_{IN}/V_{OUT} = 5V. Unless otherwise noted, the *Min* and Max specs are applied over the full operation temperature range of -40°C to +85°C, while *Typ* values are specified at room temperature (25°C).

Symbol	Description	Conditions	Min	Typ	Max	Units
INPUT, OVP (IN to OUT)						
V_{IN}	Input Operating Supply voltage		3.0		24.0	V
V_{OUT}	Output Operating Supply voltage		3.0		24.0	V
V_{UVLO}	Input /Output UVLO rising threshold	Initiates soft-start after deglitch time	2.3	2.7	2.95	V
I_{OUT}, I_{OTG}	Continuous output current				5	A
V_{OVP}	Input OVP rising threshold	$V_{IN} > V_{OVP}$ enters Fault mode; VP = GND	22.2	23.4	24.4	V
		$V_{IN} > V_{OVP}$ enters Fault mode; VP = FLOAT	12	13	14	V
V_{UVLO}	UVLO Hysteresis	Falling VIN		0.2		V
$V_{OVP-HYS}$	OVP Hysteresis	Falling VIN		0.5		V
$V_{IN-CLAMP}$	Input Clamp Voltage	I_{IN} = 10mA, T_A = +25°C	28	32		V
$R_{DSON\ (IN-OUT)}$	Switch ON Resistance	I_{IN} = 1A, T_A = +25°C		25	35	mΩ
I_{Q-IN}	Input quiescent current, Standby/Fault state	$\overline{EN}$ = High		160	210	µA
I_{DD-IN}	Input operating current	$\overline{EN}$ = Low, I_{OUT} = 0mA		160	210	µA
I_{Q-OUT}	Output quiescent current, Standby/Fault state	OTG-mode, $\overline{EN}$ = High		170	220	µA
I_{DD-OUT}	Output operating current	OTG-mode, $\overline{EN}$ = Low, No load		160	210	µA
$I_{QIN-GND(CLAMP)}$	Clamping IN quiescent current	V_{IN} = 28V; VOUT = 0V to 6V		0.3	5	mA
R_{DIS}	OUT discharge resistance	Measured from OUT to GND during discharge event		450	650	Ω
$V_{IN-OUT(Float)}$	OUT float voltage	Standby state, $\overline{FLAG}$ = high and/or $\overline{EN}$ = high; VIN = 4.5V to 16V			2	V
$V_{OUT-IN(Float)}$	IN float voltage	OTG state, $\overline{FLAG}$ = high and/or $\overline{EN}$ = high; VOUT = 4.5V to 16V			2	V
VSNS						
V_{SNS}	Regulated Output	VIN = 6V to OVP; ISNS = 0mA to 40mA; CSNS = 0.1uF;	4.7	5	5.3	V

5. KTS1675A is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

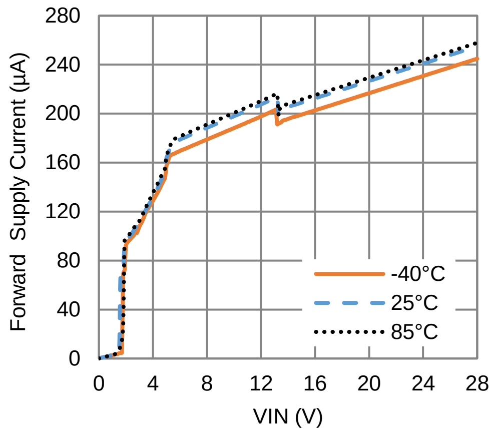
Electrical Characteristics (continued)[5]

Symbol	Description	Conditions	Min	Typ	Max	Units
TIMING CHARACTERISTICS						
t_{DEB}	Input debounce time	$V_{UVLO} < V_{IN} < V_{OVP}$, $\overline{EN}$ = low, time delay between VIN rising and $\overline{WRX}$ rising		50		ms
t_{DIS}	Discharge time	Time after debounce time $\overline{WRX}$ rising to VOUT soft-start		50		ms
t_{SST}	Soft-start time	Bidirectional IN to OUT or OUT to IN, time is from 20% to 80% of input		0.5	1.0	ms
$t_{OVP-DLY}$	Switch turn-off response time	$V_{IN} > V_{OVP}$ to VOUT stop rising		70		ns
t_{DELAY}	Logic pin enable delay: $\overline{EN}$, $\overline{FLAG}$	Time delay from $\overline{EN}$, $\overline{FLAG}$ enable/disable load switch, excluding soft-start		200		µs
DIGITAL SIGNALS						
V_{IL}	Digital Logic Thresholds; Logic input pins: $\overline{EN}$, $\overline{FLAG}$, $\overline{WRX}$	Input logic low			0.4	V
V_{IH}		Input logic high	1.1			V
V_{OL}	Output voltage: $\overline{FLAG}$, $\overline{WRX}$	Output logic low, Sinking = 1mA			0.4	V
V_{OH}		Output logic high, no load	2.6	3.25	3.6	V
R_{OH_FLAG}	Pull-up resistance: $\overline{FLAG}$,			400		kΩ
R_{OH_WRX}	Pull-up resistance: $\overline{WRX}$			200		kΩ
R_{EN}	$\overline{EN}$ Pull-down resistor			400		kΩ
ESD PROTECTION (IEC61000-4-2)						
V_{ESD}	Human Body Model (HBM)	All pins		±2		kV
	IEC61000-4-2 Contact discharge	IN pin		±8		
	IEC61000-4-2 Air gap discharge	IN pin		±15		
Thermal Shutdown						
t_{J-TH}	IC junction thermal shutdown threshold			150		°C
	IC junction thermal shutdown hysteresis			15		°C

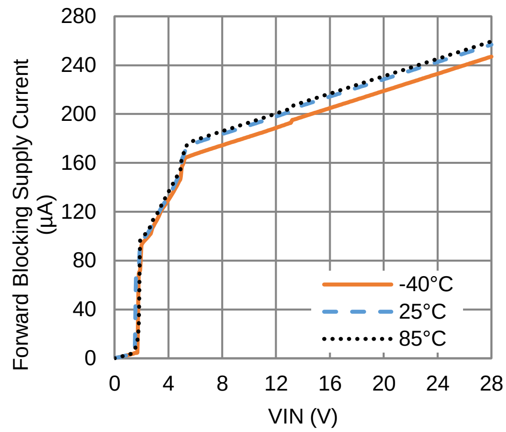
Typical Characteristics

V_{IN}/V_{OUT} = 5V, C_{IN} = 1µF, C_{OUT} = 10µF, $\overline{WRX}$ floating (high), $\overline{FLAG}$ floating (high), $\overline{EN}$ floating (low), VP floating (13V V_{OVP}), Temp = 25°C unless otherwise specified.

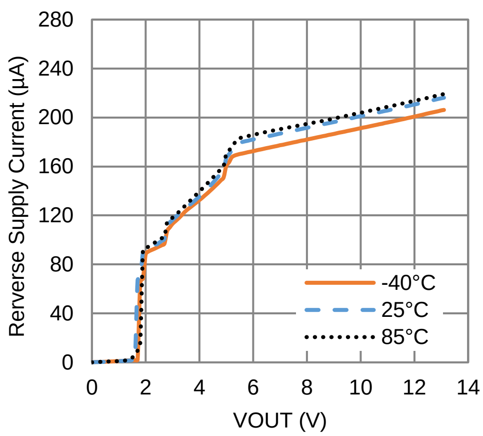
Forward Supply Current vs. VIN (Switch on)



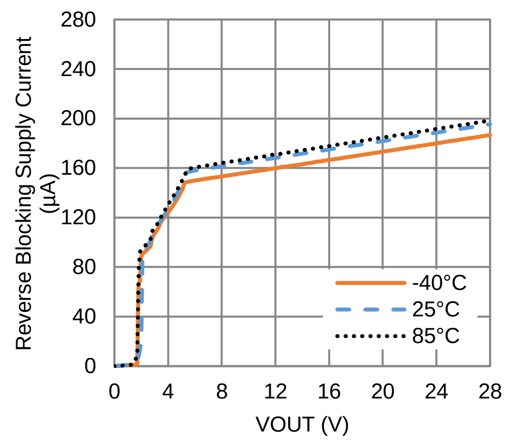
Forward Blocking Supply Current vs. VIN (Switch off, $\overline{EN}$ = high)



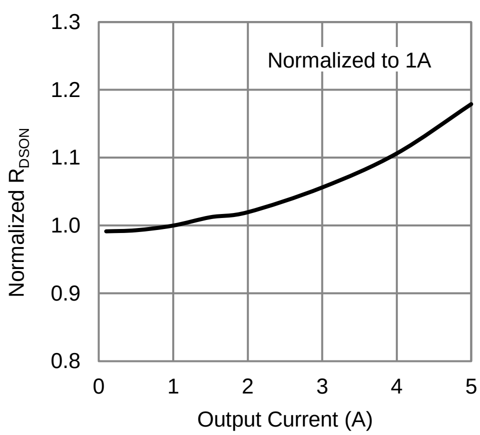
Reverse Supply Current vs. VOUT (Switch on, $\overline{FLAG}$ = low)



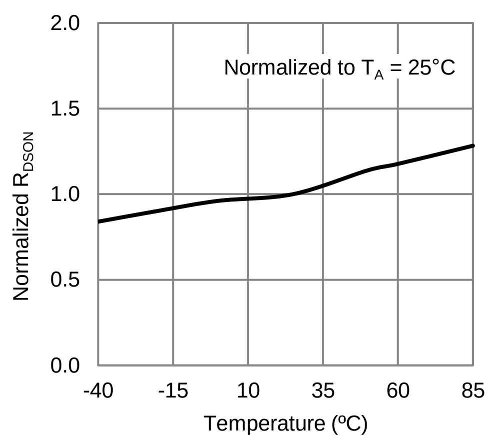
Reverse Blocking Supply Current vs. VOUT (Switch off, $\overline{FLAG}$ = high)



Normalized R_{DSON} vs Output Current (V_{IN} = 5V)



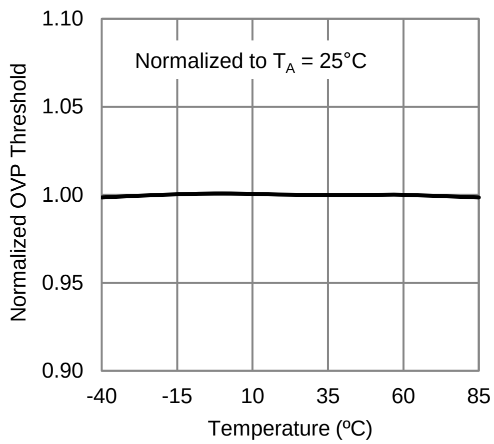
Normalized R_{DSON} vs. Temperature (I_{OUT} = 1A)



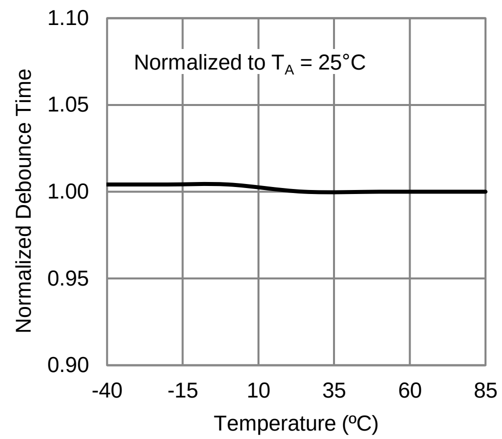
Typical Characteristics

V_{IN}/V_{OUT} = 5V, C_{IN} = 1µF, C_{OUT} = 10µF, $\overline{WRX}$ floating (high), $\overline{FLAG}$ floating (high), $\overline{EN}$ floating (low), VP floating (13V V_{OVP}), Temp = 25°C unless otherwise specified.

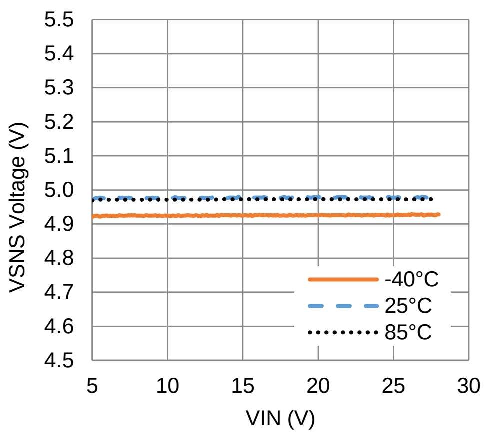
Normalized OVP Threshold vs. Temperature



Normalized Debounce Time vs. Temperature



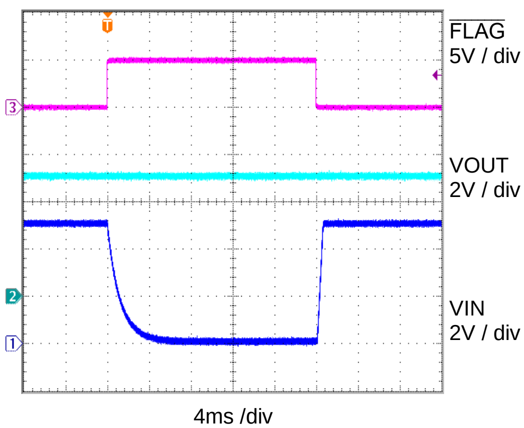
VSNS Voltage vs. VIN



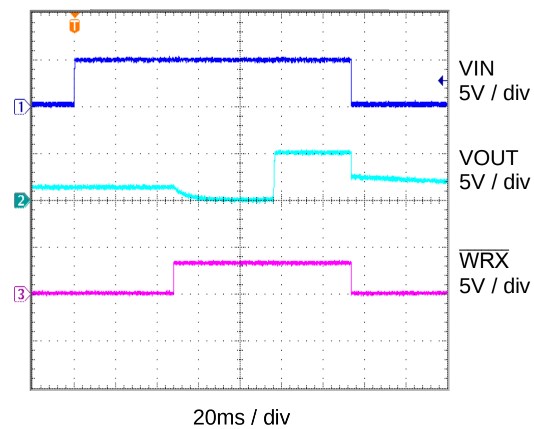
Typical Characteristics (continued)

V_{IN}/V_{OUT} = 5V, C_{IN} = 1µF, C_{OUT} = 10µF, $\overline{EN}$ floating (low), VP floating (13V V_{OVP}), Temp = 25°C unless otherwise specified.

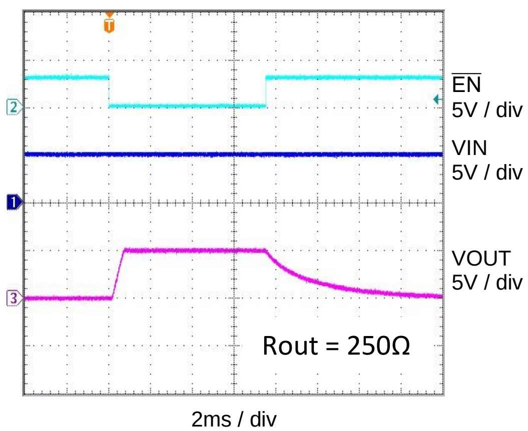
OTG Mode $\overline{FLAG}$ Turn on-off



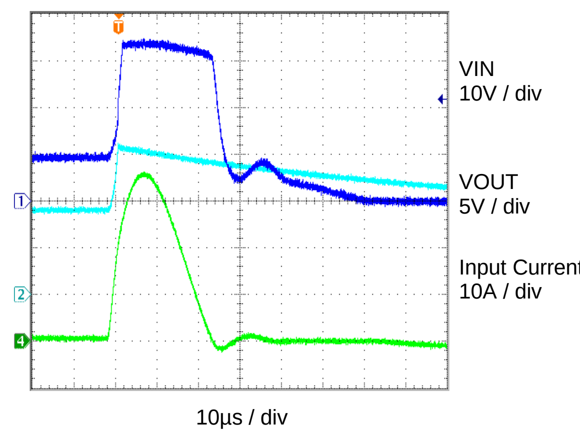
VIN 5V Insert-Remove



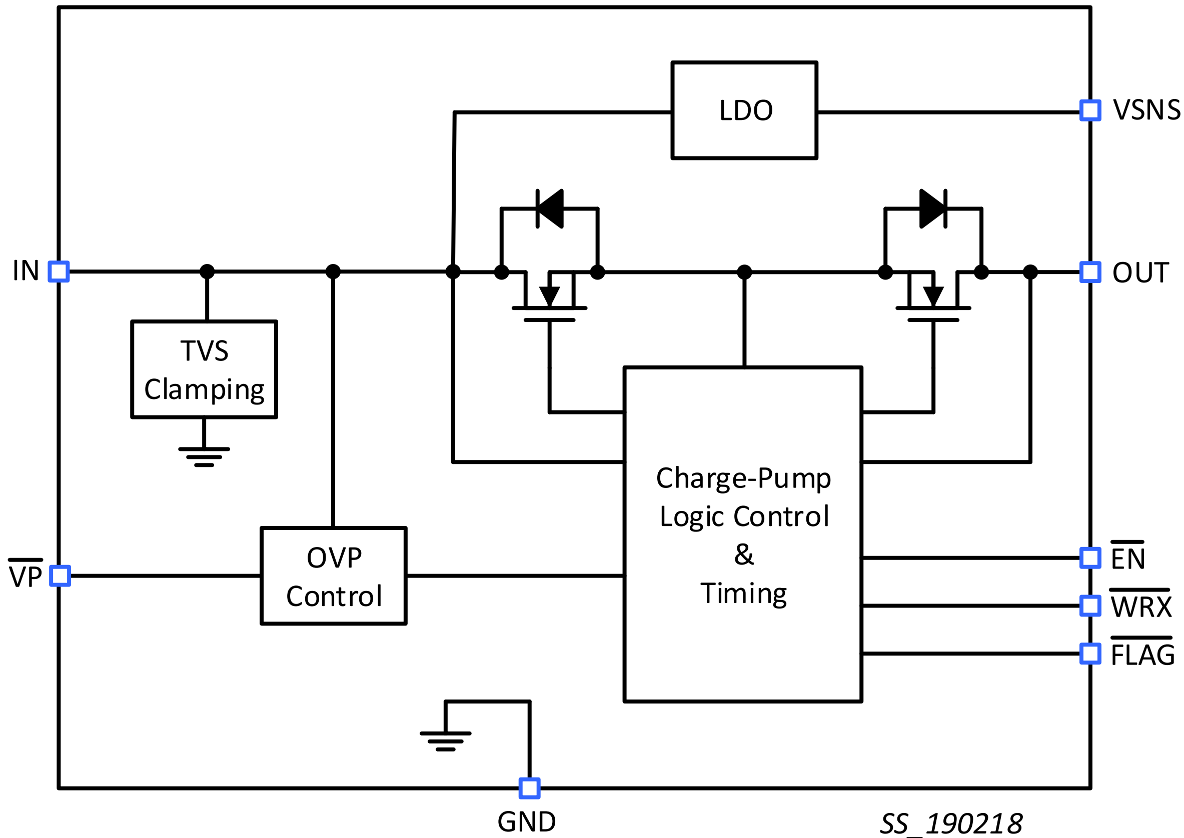
Turn on-off with $\overline{EN}$ (Slave mode $\overline{WRX}$ = $\overline{FLAG}$ = low)



Surge Transient (100V)



Functional Block Diagram



Functional Description

The KTS1675A is inserted between the power supply or charger source and the load to be protected. The KTS1675A consists of two "back-to-back" low resistance OVP MOSFET switches, under-voltage lockout protection (UVLO), over-voltage monitors and protection (OVLO), and power good output flags.

The KTS1675A overvoltage protection device features low on-resistance (R_{DSON}) internal FETs and protects low-voltage systems against voltage faults up to +28VDC. An internal clamp also protects the device from surges up to +100V. If the input voltage exceeds the overvoltage threshold, the internal FETs are turned off to prevent damage to the protected components. A 50ms debounce time built into the device prevents false turn on of the internal FET during startup. The KTS1675A also supports OTG mode where both MOSFETs can be turned-on to provide current flow from OUT to IN. With OTG mode de-asserted and the switch turned off, the KTS1675A blocks any voltage at OUT appearing at IN.

The KTS1675A features a VP selector pin, which gives the user two OVP trig level options. Connecting VP to ground, selects an OVP of typically 23.4V and when the VP is left to "FLOAT" selects and OVP of typically 13V.

Dual Input Device Operation

The addition of a wireless receiver (WRx) with an enable pin allows KTS1675A load switch to implement an equivalent 2:1 power multiplexer (PMUX), see Figure 1. When disabled, the wireless receiver withstand voltage must be greater than or equal to 24V which is the load switch maximum input operating voltage.

The load switch can transition between OFF state and OTG modes based on the input state (IN adapter and/or WRx). When the charger detects an OTG plug-in event, the transition to OTG mode is possible.

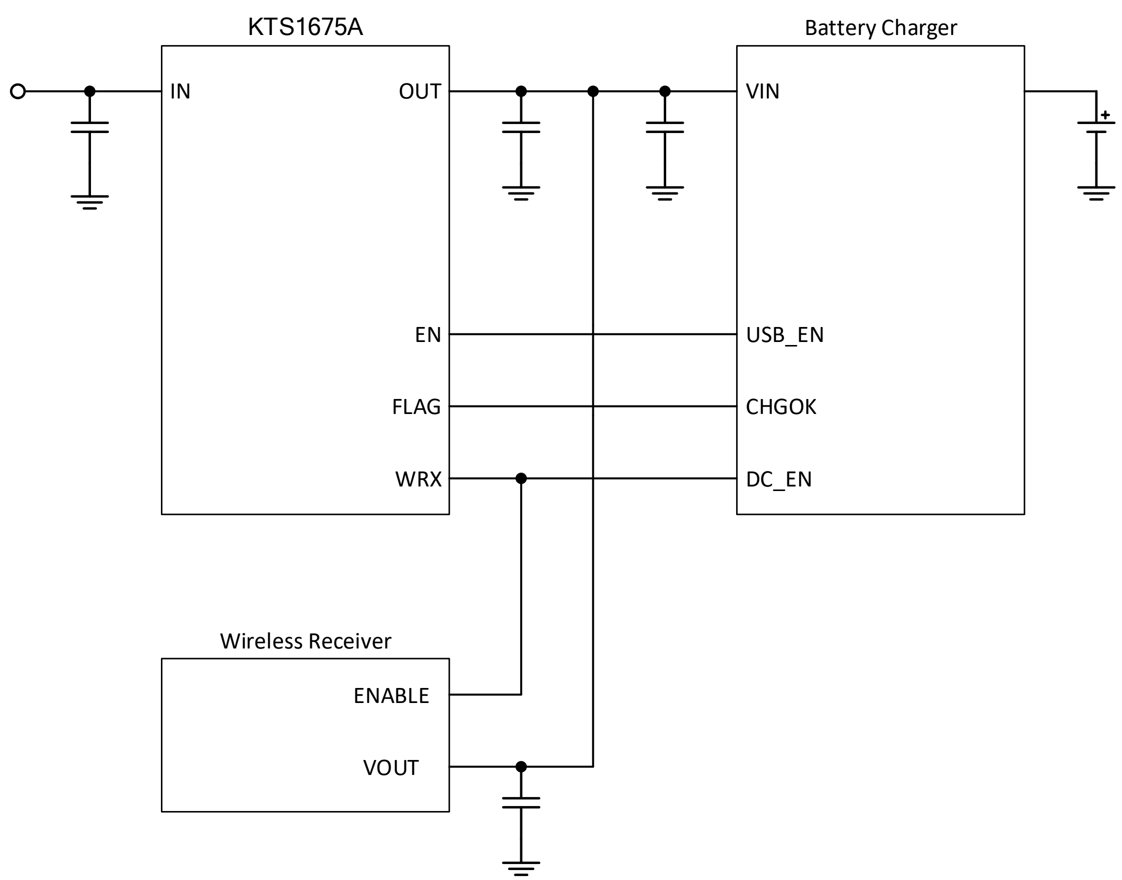


Figure 1. Dual Input Device Operation

Operation Modes

KTS1675A can operate in Slave or Autonomous modes. Slave mode allows the system (battery charger) to act as master and determine the input priority, while Autonomous mode assigns input priority to the IN power source over the wireless receiver.

Both slave and autonomous include a 50ms input debounce and 0.5ms soft-start times.

Autonomous mode includes a 50ms automatic break-before-make plus discharge period that is disabled in slave mode by grounding $\overline{\text{WRX}}$ pin.

Autonomous Mode

In Autonomous mode, after the $\overline{\text{EN}}$ pin is tied to GND, the load switch controller activates the load switch ON-State after a fixed time delay when a valid input voltage is detected from IN. Autonomous mode gives priority to the IN input.

- Charging (IN to OUT):
  - The load-switch controls input/wireless priority.
  - System interface with valid IN.
  - Charger pulls $\overline{\text{EN}}$ to LOW to allow current flow from IN to OUT.
  - After $\overline{\text{EN}}$ is pulled to LOW, $\overline{\text{WRX}}$ would become HIGH to disable wireless receiver.
  - $\overline{\text{FLAG}}$ only become HIGH when OTG requirements are met (OUT is valid while IN is LOW).

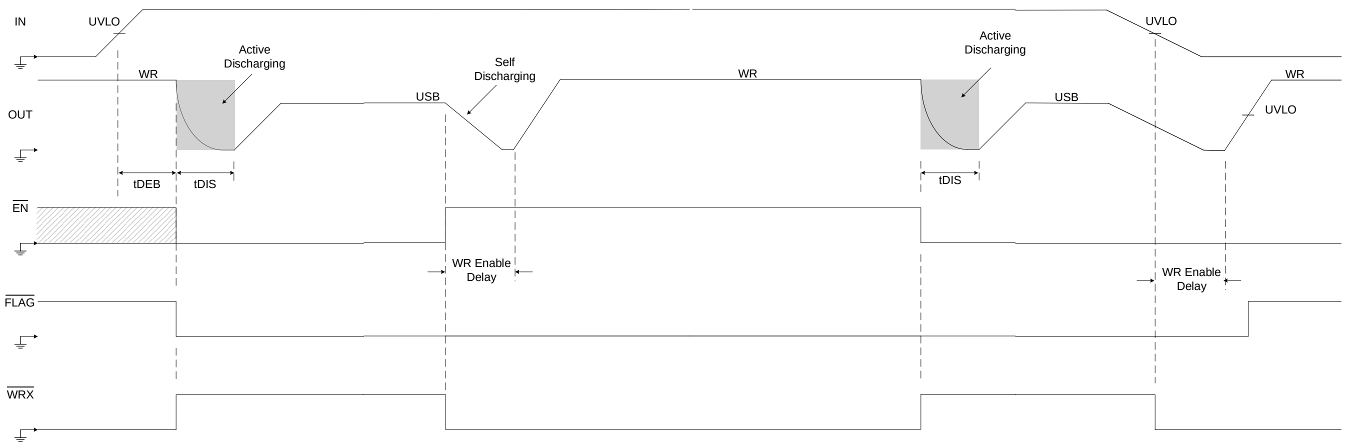


Figure 2. Autonomous Mode Charging ($\overline{\text{EN}}$ is is pulled to LOW before tDEB expires)

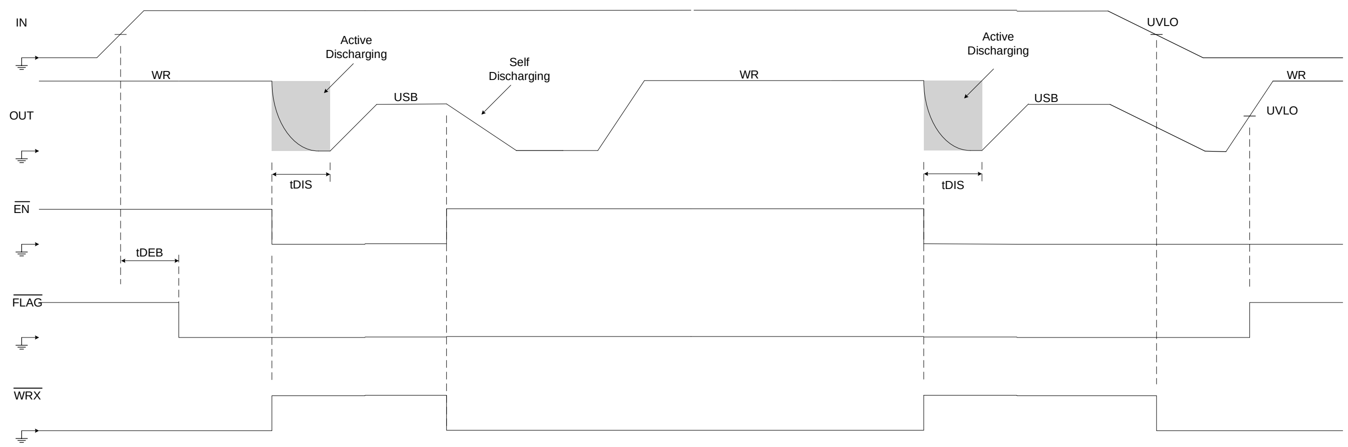


Figure 3. Autonomous Mode Charging ($\overline{\text{EN}}$ is pulled to LOW after tDEB expires)

- OTG (OUT to IN):
  - A valid voltage is detected from OUT, and IN is below UVLO.
  - $\overline{\text{FLAG}}$ becomes HIHG since OTG requirements are met.
  - Charger pulls both $\overline{\text{EN}}$ and $\overline{\text{FLAG}}$ to LOW to allow current flow from OUT to IN.
  - After $\overline{\text{FLAG}}$ is pulled to LOW, $\overline{\text{WRX}}$ would become HIGH to disable wireless receiver.

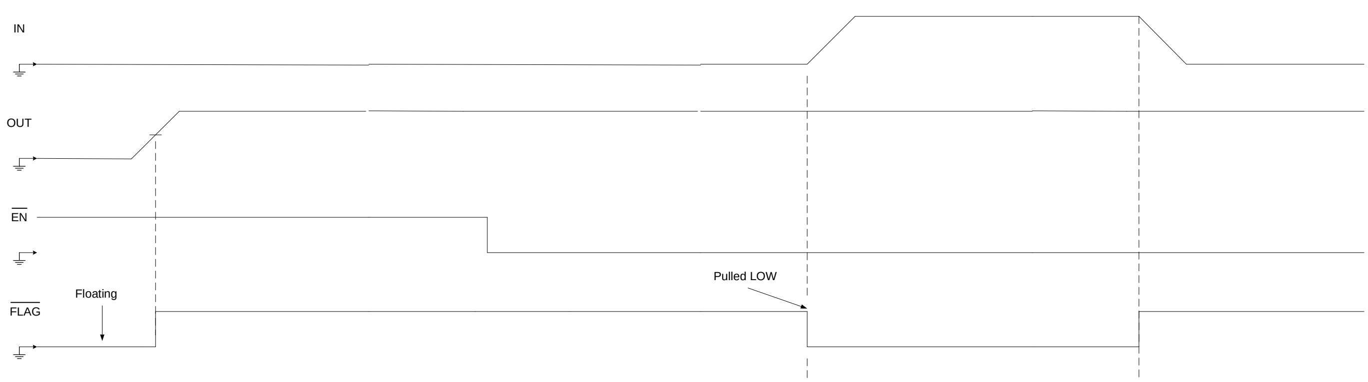


Figure 4. Autonomous Mode OTG

Slave Mode

In Slave mode, both $\overline{\text{FLAG}}$ and $\overline{\text{WRX}}$ pins are tied to GND. The system (battery charger) acts as master and disables the wireless receiver and activates the load switch On-State via the $\overline{\text{EN}}$ pin. Slave mode allows the system (charger) to assign the priority of the input power source when both power sources are active.

- Charging (IN to OUT):
  - System interface with a valid IN:
  - The wireless receiver should be turned off by the charger before performing charging through KTS1675A.
  - Pull $\overline{\text{EN}}$ to low to turn on the switch to allow current flow from IN to OUT.

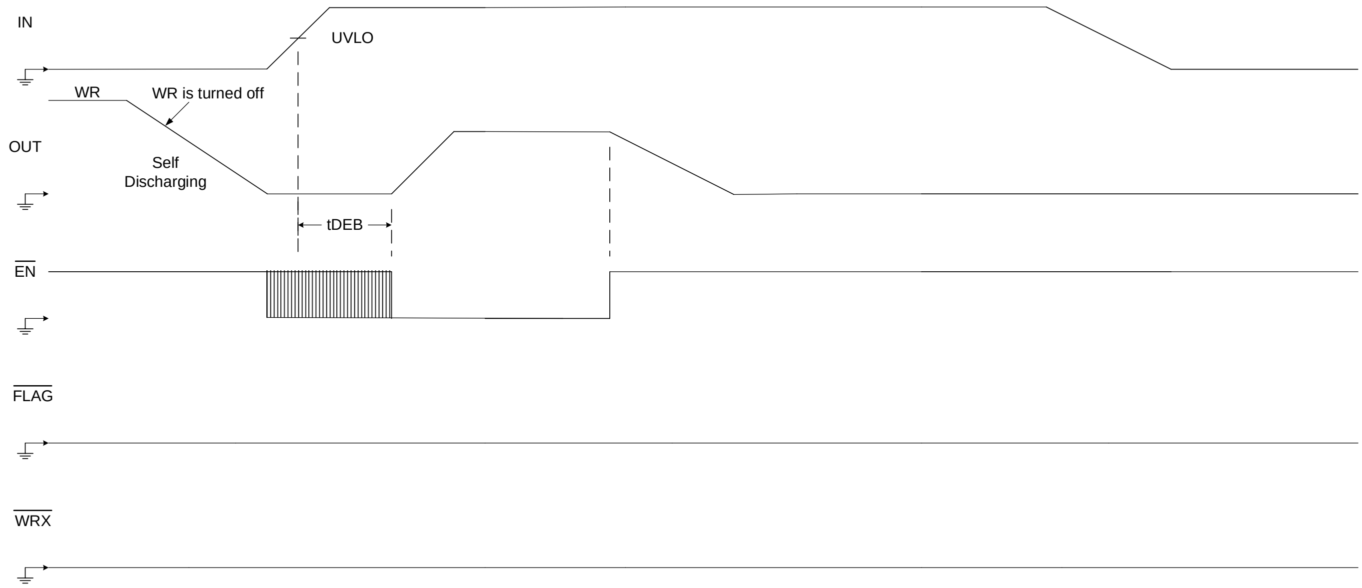


Figure 5. Slave Mode Charging ($\overline{EN}$ is pulled to LOW by charger before tDEB expires)

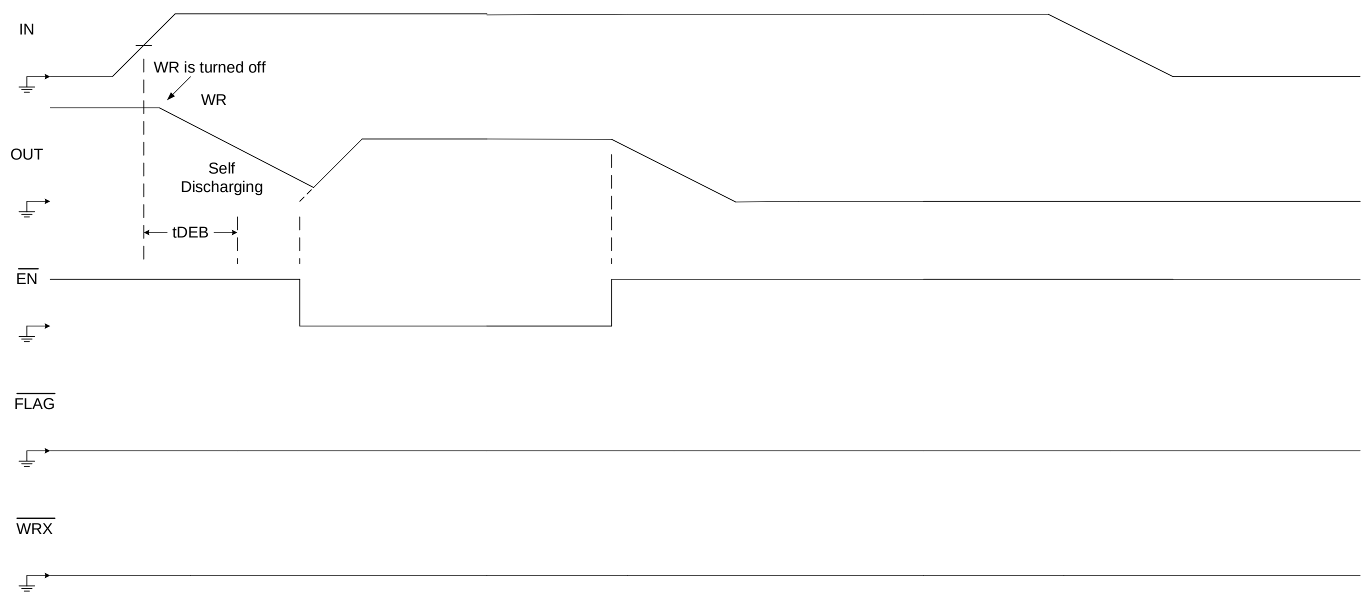


Figure 6. Slave Mode Charging ($\overline{EN}$ is pulled to LOW by charger after tDEB expires)

- OTG (OUT to IN):
  - Once OUT is valid while IN is not, charger pulls $\overline{EN}$ to LOW to allow current flow from OUT to IN.

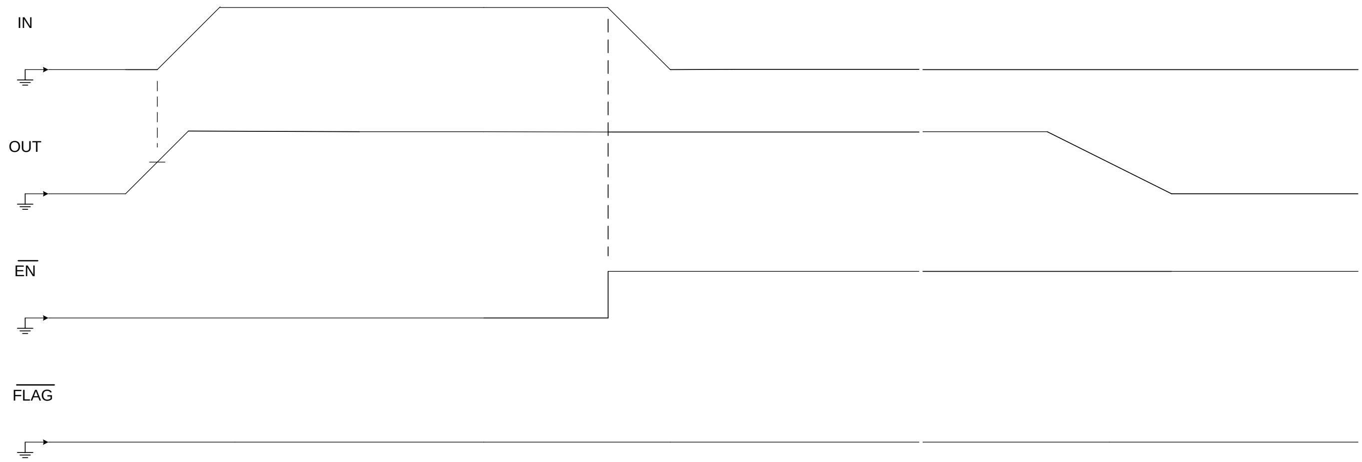


Figure 7. Slave Mode OTG ($\overline{EN}$ is pulled to LOW before Vin ramps up)

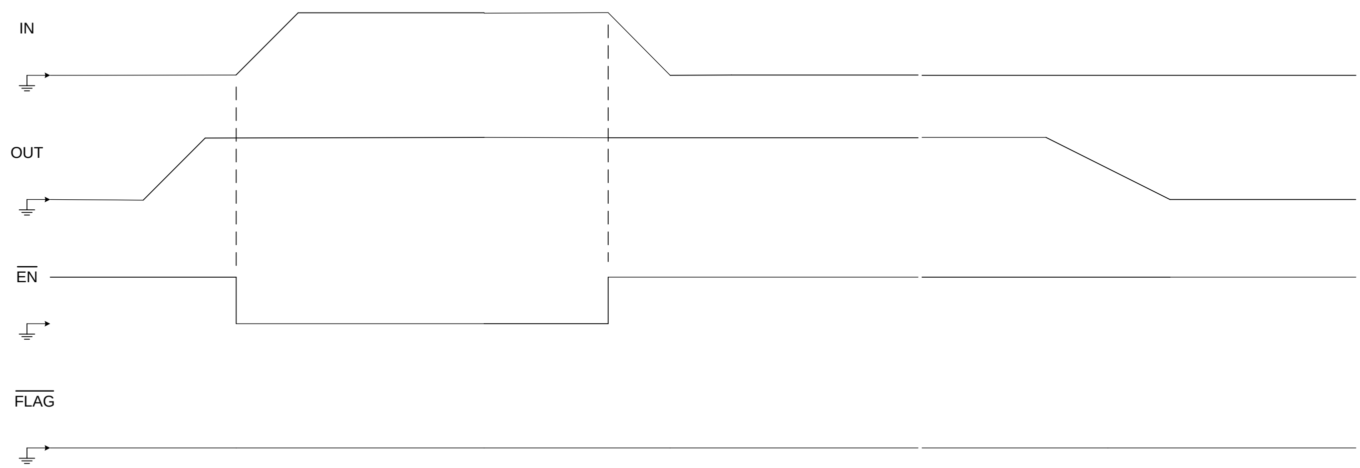


Figure 8. Slave Mode OTG ($\overline{EN}$ is pulled to LOW after Vin ramps up)

Input Surge Protection

The device must withstand up to 100V surge voltage applied from the IN pin to ground pin. The surge may be applied to the load switch in the on or off states. The surge waveform is compatible with the IEC 61000-4-5 specification, R_{SOURCE} = 2.0Ω, 1.2/50µs waveform.

Over-voltage Protection

In normal operation, the OVP switch acts as a slew-rate controlled load switch, connecting and disconnecting the power supply from IN to OUT.

When the voltage on the input exceeds the selected programmed over-voltage trip point, the device immediately turns off the internal OVP switch, disconnecting the load from the abnormal voltage, preventing damage to any downstream components.

The OVP trip point can be selected by the VP pin. Connecting to GND gives a typical 23.4V trip point and allowing VP to float, typical 13V.

Soft-start

In-rush current is minimized by a soft-start (t_{SST}) which occurs during activation of the load switch. Soft start occurs when the switch is enabled, either in slave mode or autonomous mode.

OTG

OTG could be performed after the charger detects an OTG plug-in event, around 5V is applied to the OUT pin, and the IN pin is tied to an OTG load.

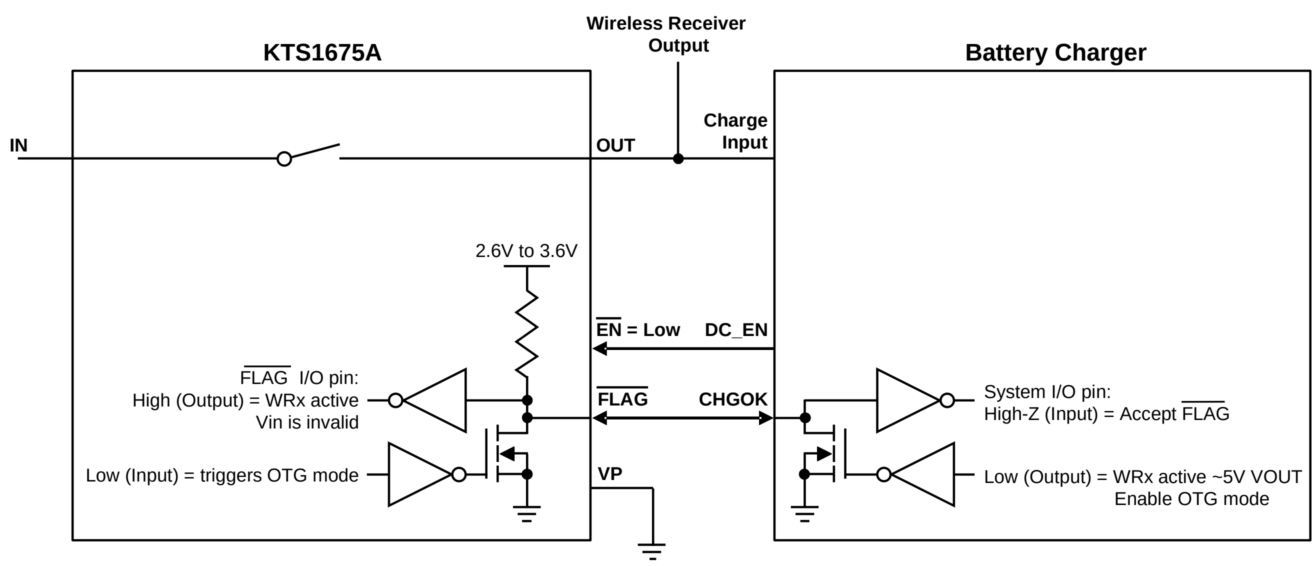
Bidirectional Blocking

The KTS1675A features bidirectional blocking. When IN pin voltage is below the input start-up voltage and $\overline{\text{FLAG}}$ is high (OTG mode disabled), the switch between IN and OUT is open and the internal diodes of the two MOSFET switches are back-to-back, thereby blocking any reverse current. This is also true when the device is in OVP mode.

$\overline{\text{FLAG}}$ logic

The $\overline{\text{FLAG}}$ pin is a bidirectional input/output pin that controls the transition to and from OTG modes while in autonomous mode.

When IN is disconnected (floating) and a valid OUT voltage is detected, the $\overline{\text{FLAG}}$ pin serves as an output signal and $\overline{\text{FLAG}}$ = logic high. Subsequently, the load switch can be activated by toggling the $\overline{\text{FLAG}}$ = logic low, which triggers OTG by transitioning into the ON-state.



IN	OUT	$\overline{\text{FLAG}}$	CHGOK	Load - Switch Behavior ($\overline{\text{EN}}$ = Low)
< VUVLO	>VUVLO	High	Hi-Z	Load switch = OFF and OTG mode can be enabled On/off state of WRx determined by battery charger
= VOUT	= VOUT	Low	Low	Load switch = ON, OTG mode(s) enabled On/off state of WRx determined by battery charger
>VUVLO	Low	Low	X	Load switch = OFF ($\overline{\text{EN}}$ = High), OTG mode not allowed

Figure 9. $\overline{\text{FLAG}}$ Logic

VSNS Indication

VSNS is a regulated output of 5V typical. It can support 5V@40mA to external loads. Once IN exceeds UVLO, it starts to output. It will be turned off when an OTP event was detected. Though, it is supposed to be able to source up to 40mA without hitting over-current protection, caution is still needed to avoid too much power consumption caused by too big voltage drop from IN to V_{SNS}.

Below is the timing diagram illustrating VSNS's behavior.

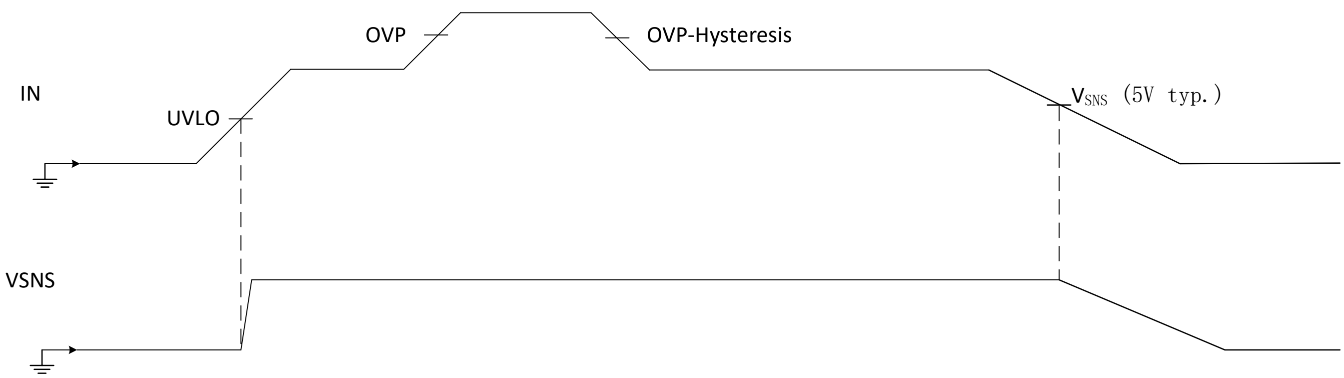


Figure 10. Timing Diagram Illustrating VSNS's Behavior

Thermal Protection

The KTS1675A features thermal shutdown to prevent the device from overheating. The internal FETs turn off when the junction temperature exceeds +150°C (typ). The device exits thermal shutdown after the junction temperature cools by 15°C (typ) hysteresis.

Applications Information

Input Capacitor

A 1μF or larger capacitor is typically recommended for C_{IN}. C_{IN} should be located as close to the device IN pin as practically possible. 50V rated capacitors are generally good for most OVP applications to support any surge transient voltage.

Output Capacitor

The soft-start function provides a slow turn-on that allows the KTS1675A to charge large output capacitors with minimum in-rush current. It is recommended to bypass OUT with a 1μF minimum ceramic capacitor.

VSNS Capacitor

A 0.1μF or larger capacitor is typically recommended for $C_{VSNS.}$ In order to reduce the start up inrush current, it is recommended to bypass VSNS with a 1μF maximum ceramic capacitor

ESD Test Conditions and Human Body Model ESD Protection

The KTS1675A fully supports the IEC61000-4-2, (Input pin, 1μF mounted on board). In Air condition, V_{IN} has a ±15kV ESD protected input. In Contact condition and air-gap condition, V_{IN} has ±8kV ESD protected input.

Recommended PCB Layout

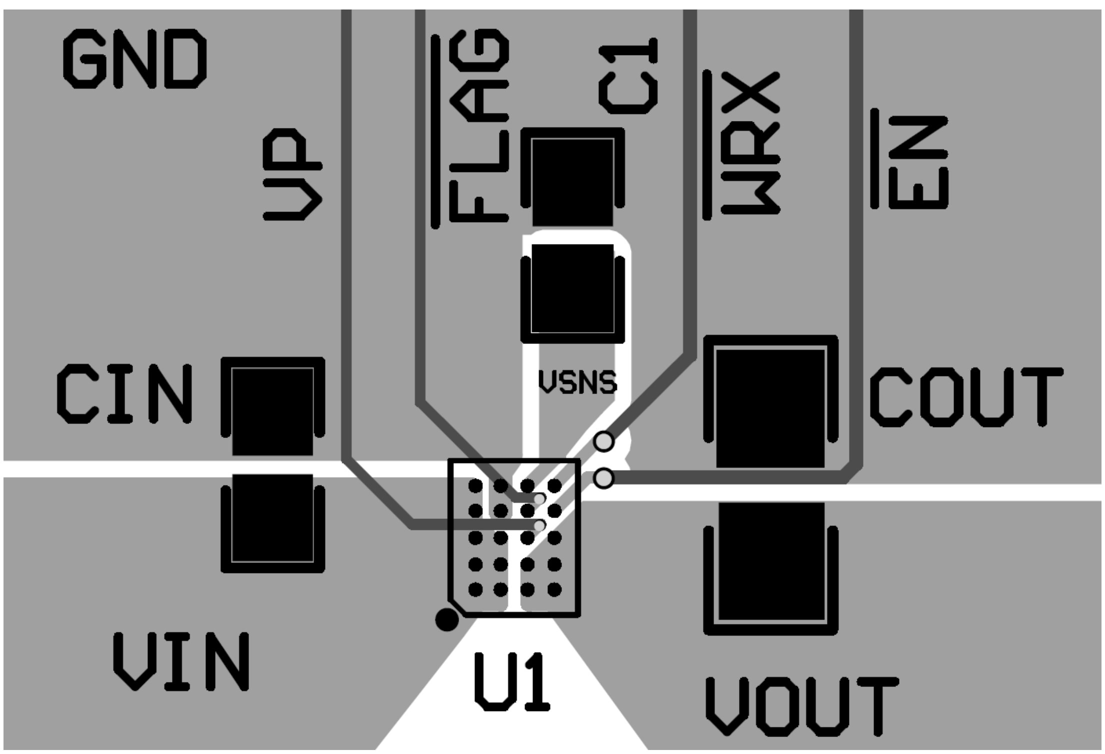
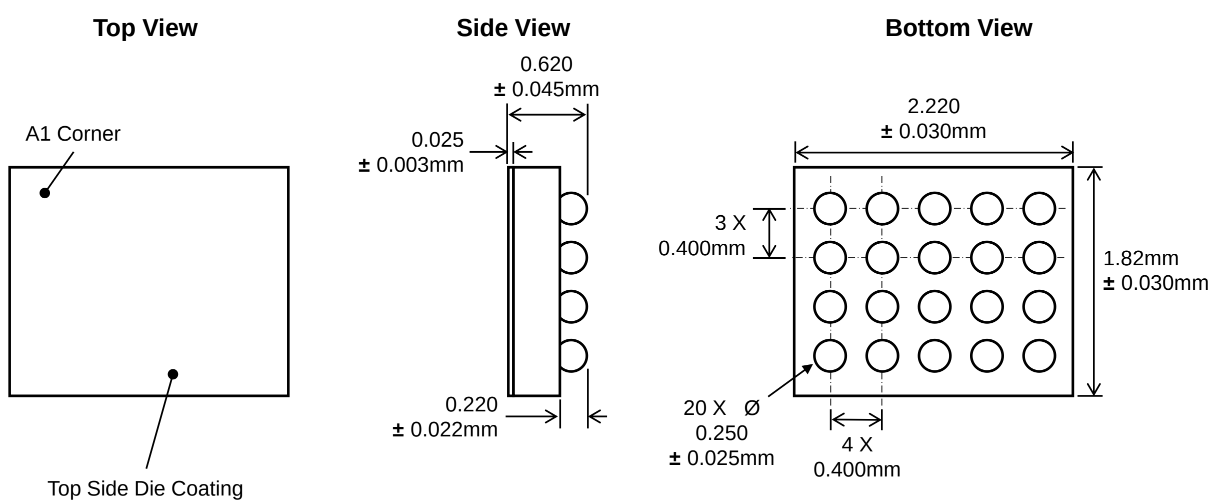


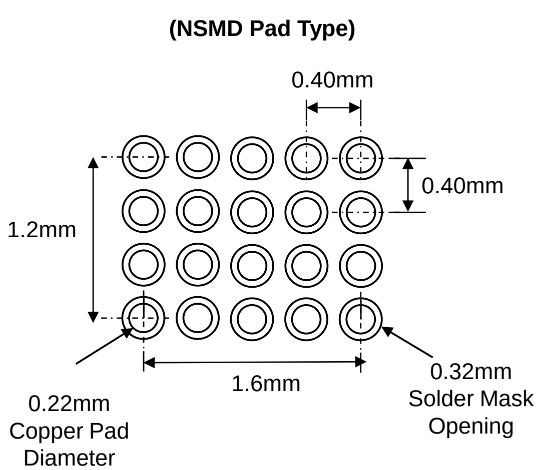
Figure 11. Recommended PCB Layout

Packaging Information

WLCSP54-20, 2.22mm x 1.82mm x 0.62mm



Recommended Footprint



* Dimensions are in millimeters.