USB Type-C / DisplayPort 1.4 MST Hub (DSC)

Features

- USB Type-C DisplayPort Alt-mode de-mux
  - Simultaneous USB3.2 Gen2 and 2 lanes DP1.4a input OR 4 lanes DP1.4a input
  - Flip option for connector plug orientation
  - DP lane swap and polarity swap
- DisplayPort® (DP) ver.1.4a compliant receiver
  - Link rate 1.62 / 2.74 / 5.4 / 8.1Gbps
  - 1, 2, or 4 lanes configuration
  - MST up to 6 streams (compressed /uncompressed)
  - FEC Decode
  - DSC Transport & Decode
  - AUX CH 1 Mbps
  - HPD_OUT
  - Adaptive receiver equalization
  - TPS4 EQ Phase LT support
  - Scrambling of main link data
  - De-spreading of link frequency
  - Video Stream Handling
    - RGB/ YCC 444/422/420 pixel format up to 16 bpc
    - Up to 1080 Mpix/sec dual pixel path
  - DPCD
    - DPCD data structure revision 1.4
    - DSC support capability & control
    - FEC capability & control
    - SST Split SDP capability
    - VSC_EXT_SDP for VESA & CTA
    - Protocol converter capability & control
    - Virtual DP Peer Device capability & control
    - CEC tunneling over AUX
  - Chainable SDP packets (2KB or more metadata per stream)
  - Adaptive Sync SDP
  - PPS SDPAudio stream handling
    - Non-HBR Compressed Formats
      - 2/8 ch layouts
      - Up to 192kHz sample rates
      - Dolby Digital, Digital+, Atmos
  - HBR Audio Formats
    - 8 ch layout
    - Up to 1536kHz sample rates
    - Dolby TrueHD, Atmos, DTS Master
    - LPCM Formats
    - 2/8/16/32 Ch
    - Up to 192kHz sample rates
    - 3D LPCM, speaker allocation & mapping
  - OneBit DSD Formats
    - 2/8 ch
    - Single & Double Rate
    - 12288 kHz sample rates
  - DST DSD Formats
    - Single/Double rate
    - Up to 22579.2kHz
  - Audio InfoFrame/ ACP/ ISRC/ Audio Metadata DI packets
- Triple DP1.4a / HDMI2.0b (DP++) transmitters
  - DP mode
    - Lane count, Link rate conversion
    - Link rate 1.62 / 2.74 / 5.4 / 8.1Gbps
    - 1, 2, or 4 lanes configuration
    - DSC stream transport with FEC Encode
    - MST up to 6 streams (compressed / uncompressed)
    - AUX CH 1 Mbps
    - 3.3V HPD_IN
  - HDMI mode
    - TX1 & TX3: VML AC coupled HDMI
    - TX2: CML DC-coupled HDMI
    - No External Level shifters needed
    - 600 MHz maximum TMDS character clock
    - TMDS character-clock divide_by_4 mode
    - HPD_IN (5V Tolerant)
    - DDC CH (5V Tolerant)
- HDMI 2.1 Features
  - Through 6GHz TMDS Mode
  - Supports 4k120Hz,4:2:0, 8bpc with Adaptive Sync to VRR conversion
  - Dynamic HDR Metadata through Extended Metadata Packet
  - Supports VRR, FVA, QMS, QFT, ALLM
  - Scrambler for DP/HDMI output
  - Programmable signal amplitude and edge rate control
  - Programmable pre-emphasis control
  - Pixel format RGB / YCC 444/422/420
  - Deep color up to 16 bits per color
  - 3D video timings
  - CEC support – snooping, tunneling
  - SCDC read request handling
  - Metadata handling
  - Conversion to DVI output
  - Link power management

Features (continued)

- USB3.2 compliant re-timer
  - 5Gbps and 10Gbps support
  - Spread spectrum clocking
  - LFPS polling and processing
  - Lane polarity inversion
  - Bit level re-timer for SS mode
  - SRIS (Separate Reference Clock Independent SSC) for SSP mode
  - Adaptive Receiver Equalization
  - Multi-tap FIR EQ Transmitter Emphasis
- Video processing
  - MST to SST conversions or pass-through
  - SST lef-right separation
  - Color space conversion from RGB to YCC
  - Colorimetry support: BT2020, BT709, BT601, and Adobe RGB
  - Color bit depth expansion (10 to 12 bits) 16 bits per color pass through
  - DP to HDMI Stereoscopic 3D Transport
  - Frame sequential to stacked top-bottom conversion
  - Pass through of other 3D formats
  - Programmable coefficient 3x3 matrix
    - Programmable input offset
    - Programmable output offset
    - Programmable output clipping levels
  - Chroma down sampling
    - 5-tap H & V FIR filters with programmable coefficients
    - 12 bits per color input width
    - 12 bits per color output width
    - YCbCr444 to YCbCr420 conversion
    - YCbCr444 to YCbCr422 conversion
  - Pass through for YCbCr444/422/420
  - Dual DSC1.2A stream decoding
  - 1/2/4 Slice DSC1.2Aa RGB/YCC444/422/420 10-b format support
  - FEC decoding / encoding
  - Video Horizontal blanking expansion
  - Pixel stream de-skewing
  - Adaptive Sync Video
- Max video resolution and color depth on DP output uncompressed
  - 5K3K60Hz, RGB/YCbCr444, 8 bpc
  - 8K4K60Hz, YCbCr420 up to 8 bpc
  - 4K2K120Hz, RGB/YCbCr444, 8 bpc
- Max video resolution and color depth on DP output compressed (DSC)
  - 8K4K60Hz, RGB/YCC444 up to 8 bpc
  - 5K3K60Hz, RGB/YCbCr444, 12 bpc
  - 4x 4K2K60Hz, RGB/YCbCr444, 8 bpc
- Max video resolution and color depth on HDMI TX
  - 4Kp60Hz, RGB/YCbCr444, 8 bpc
  - 4Kp60Hz, YCbCr420, up to 16 bpc
  - 4Kp30Hz, RGB/YCbCr444, up to 16 bpc
- Audio processing
  - Audio stream forwarding from DP RX to HDMI TX
  - Conversion to I2S or TDM audio output (8 CH)
  - Conversion to SPDIF audio output (2CH)
- HDCP support
  - HDCP1.3 to HDCP1.4 Repeater function
  - HDCP2.3 to HDCP1.4 Repeater function
  - HDCP2.3 to HDCP2.3 Repeater function
  - Read- protected embedded HDCP keys
- Enhanced security
  - Encrypted on-chip key storage
  - RSA-2048bit signed application firmware
  - Secure Boot & In-system Programming
  - Test, debug ports deactivation
- Metadata handling
  - HDMI TX DVI/HDMI mode setting (DPCD register)
  - YCbCr444-420 conversion (DPCD register)
  - IEC60958 BYTE3 channel status overwrite
  - CTA861G INFO FRAME generation
  - CTA861.3 HDR and Mastering InfoFrame
  - Chainable VSC_EXT SDP packing format
- ARM processor and peripheral controllers
  - ARM Cortex M3 core
  - SPI controller
  - I2C master, slave controller
  - On-Chip, RAM, ROM, OTP
- Device configuration options
  - Application FW stored in SPI flash
  - AUX CH, I2C host interface
- Internal video pattern generator
  - Configurable through vendor specific DPCD registers
- EMI reduction support
  - Spread spectrum for DP input, output
  - Scrambler for DP and HDMI outputs
- Low power operation
  - 860mW nominal operation with retimer
  - 700mW nominal operation without retimer
  - Under 10mW Standby operation
- ESD specification
  - ESD: ±2kV HBM, 500 V CDM
- Package
  - 289 LFBGA (12 x 12mm)
  - Halogen free Halogen free RoHS and Green Compliant
- Power supply voltages
  - 1.8V Analog and I/O, 0.95V Analog and core

Description

The KTM5030 is an advanced DisplayPort1.4a MST hub with an integrated USB type-C de-multiplexer, targeted primarily for Mobile Notebook accessory and display applications. This device functions as a multi-stream audio-video splitter and protocol converter with an HDCP1.x/ HDCP2.3 repeater supporting both compressed (DSC) and uncompressed AV streams.

KTM5030 has a DP alt-mode capable USB Type-C Upstream Facing Port (UFP). The four high speed lanes of UFP can receive DP1.4a MST audio-video and USB3.2 Gen2 data streams simultaneously. The input lane mapping is flexible and meets standard DP or the USB Type-C connector with flip orientation requirements. The incoming DP and USB signals are de-multiplexed, retimed, and transmitted on the Downstream Facing Ports (DFP). The KTM5030 consists of three AC coupled DP/DP++ or DC coupled HDMI/DVI DFPs, each with four high-speed lanes and one USB port with USB3.2 TX and RX pair. The Stream Routing Logic in KTM5030 allows flexible routing of incoming DP MST stream converted into any combination of MST or SST streams on any of the DFP video ports with link rate and lane count change option. Also, the SST stream can be replicated on two or more DFP ports. In addition, the DP SST stream can be converted into a HDMI or DVI output (TMDS signal format).

The combo receiver in KTM5030 supports all DP standard data rates up to HBR3 (8.1 Gbps/lane) and USB3.2 Gen1 (5.0 Gbps) and Gen2 (10.0 Gbps). The dual mode (DP++) transmitters support DP standard data rates up to 8.1 Gbps/lane and TMDS data rates up to 6.0 Gbps/lane. The side-band channel uses 1.0 Mbps Manchester-coded AUX signaling for DP and DDC signaling up to 100kbps for the HDMI interface.

KTM5030 is capable of processing up to six DP audio-video streams compressed or uncompressed. FEC decoding and encoding is employed for the reliable reception and transmission of DSC1.2a compressed streams. These streams can be part of one single large video timing or six independent video timings from a single source with corresponding independent multi-channel audio. The highest video timing per stream and the number of streams transported is limited by the DP1.4a and HDMI2.0 link bandwidth. When the received DP MST stream is in DSC1.2a compressed format, KTM5030 can decode the streams (max two streams) or pass through to the downstream sink or to another cascaded KTM5030 device. If a DP source sends an 8k4k60Hz RGB/YCC444 DSC1.2a encoded video as four 4k2k60Hz MST, then two KTM5030 devices are needed to decode all four streams. KTM5030 supports both RGB 444 and YCC444/422/420 video pixel encoding formats with a color depth up to 16 bpc (bits per component or 48 bits per pixel). It has a pixel processing unit capable of video pixel encoding format conversion from RGB444 to YCC444 with bit depth expansion and down scaling from YCC444 to YCC422/420. Pixel format conversion along with horizontal blanking expansion improves interoperability and smooth rendering of CVT video timings from a mobile PC on a consumer displays such as TVs and projectors which supports only CEA timings.

KTM5030 processes High Dynamic Range (HDR) video content specified in BT601, BT709, BT2020, BT2100 , Adobe RGB colorimetry format with the proper metadata conversion from DP to HDMI. It also offers secure reception and transmission of high bandwidth digital audio and video content with HDCP1.x or HDCP2.3 content protection. As a branch device KTM5030 functions as a HDCP1.x and HDCP2.3 repeater between the DP source and DP or HDMI sink.

KTM5030 uses an external 25 MHz reference clock for its operation. The reference clock can be generated from a 25MHz crystal or from an external source. It has a 300MHz ARM Cortex M3 CPU with on-chip memories for code and data storage. The peripheral subsystem includes SPI, UART (debug only), and I2C master, slave interfaces. An internal Power-On Reset (POR) circuit senses the voltage on the reset input and provides the chip reset during system power-up. The KTM5030 uses an external 16 Mbit SPI flash memory for storing the RSA-2048 signed application firmware with fail-safe recovery. At boot up, the CPU goes through a secure boot process authenticating the application code image stored in the SPI flash. It supports both standard mode and quad mode SPI operation. Firmware update for the SPI flash is done securely through the DP AUX_CH or I2C host interface (Secure In-System-Programming).

Table 1. Part Numbers

Features	KTM5030
Input	USB-C (DP alt-mode) (DP 4 lanes OR 2 lanes DP and 2 lanes USB3.2)
Outputs	3x DP++ (DP or HDMI) 1x USB3.2
USB De-mux & Re-timer	Yes
HDCP2.2	Yes
HDR, Pixel Processor	Yes
DSC & FEC	Yes
Package	LFBGA 12x12mm / 0.65mm pitch

Applications

The target applications of the KTM5030 are:

- Mobile PC docking stations
- Dongles
- MST video hubs
- AR / VR devices
- High end displays such as digital signage
- Daisy-chain monitors

DisplayPort and USB Type-C are the prominent interfaces in these applications and the KTM5030 offers the highest performance at the optimum bill of material cost.

Docking Station Application

In a mobile docking station topology, the KTM5030 is part of a larger system which has a system controller such as TCPC, USB hub, etc. The docking station can be a traditional dock with a custom connector or a travel dock with a USB Type-C tethered cable. The audio-video interface between the notebook and the docking station is either DP or DP Alt-Mode over USB Type-C. The KTM5030 is an ideal device for a Type-C docking station where it can function as a Type-C Port Manager (TCPM) along with an external TCPC device (e.g. Kinetic MCDP9000 TCPC). It is designed with integrated features such as a USB-C de-mux, a video hub, a protocol converter, and an HDCP repeater in a single chip. The downstream video ports can be configured as DP1.4a or HDMI2.0 depending on the requirements.

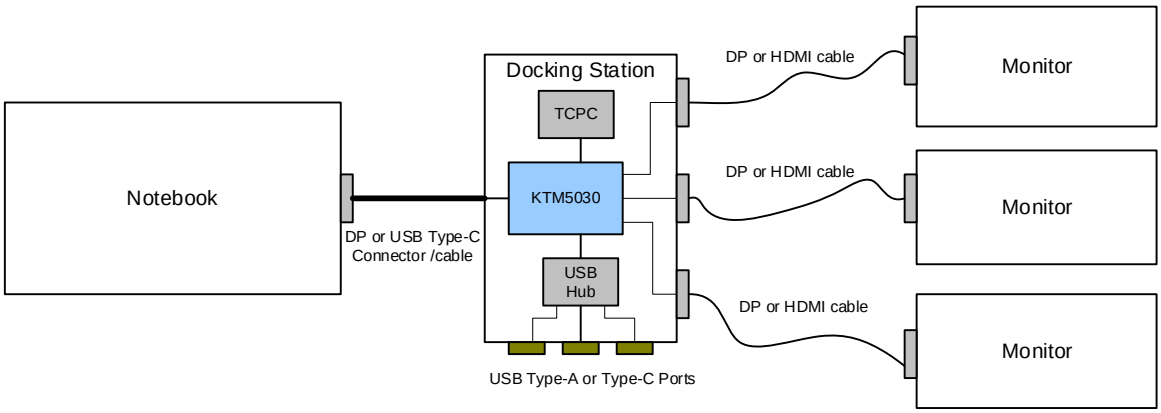


Figure 1. KTM5030 Docking Station Use Case

Daisy-Chain Monitor / Signage Application

A daisy-chain monitor or signage featuring the USB Type-C connector supporting the DP Alt-mode requires a USB Type-C de-mux and a DP MST hub device with two or more video outputs. KTM5030 is an ideal fit for such applications where it can receive the USB and multiple video streams simultaneously. It then routes one of the video stream to the internal SoC and the remaining streams to the downstream units. In this use case, the KTM5030 can support two 4K60Hz displays without DSC or up to four 4K60Hz displays with DSC.

For a Large Format Display Application, such as a 5x5 video wall configuration, KTM5030 can support 25 or more daisy chained displays.

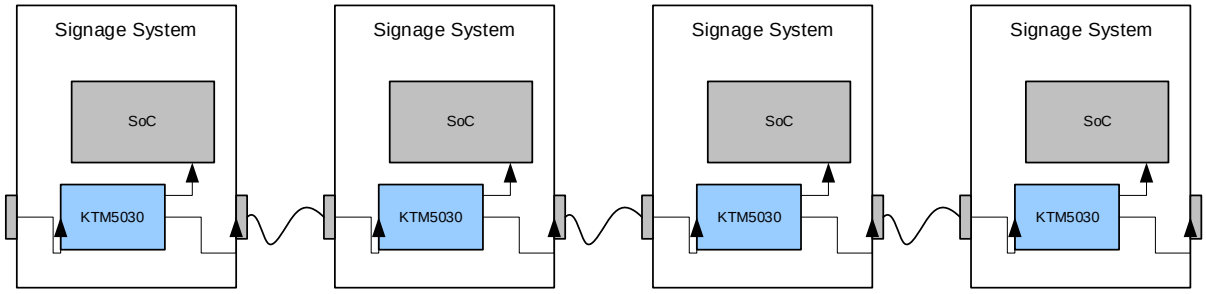


Figure 2. KTM5030 Digital Signage Use Case

AR/VR Application

The current AR/VR head mount displays use a video splitter device for routing the video from the graphics source to the dual OLED panels. Future designs are targeting higher video resolutions, refresh rates, and low latency. The KTM5030 is suitable for such designs; it can deliver up to 2x 2560x2160 @120 Hz without DSC or up to 2x 3860x2160@ 90 Hz with DSC. Additionally, the KTM5030 can generate a global frame synchronization signal for synchronizing the video with the sensor inputs. Also it can deliver up to 8CH compressed or LPCM audio through the I2S or TDM format to audio codec for the best quality audio experience.

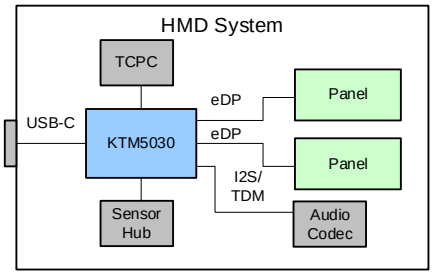
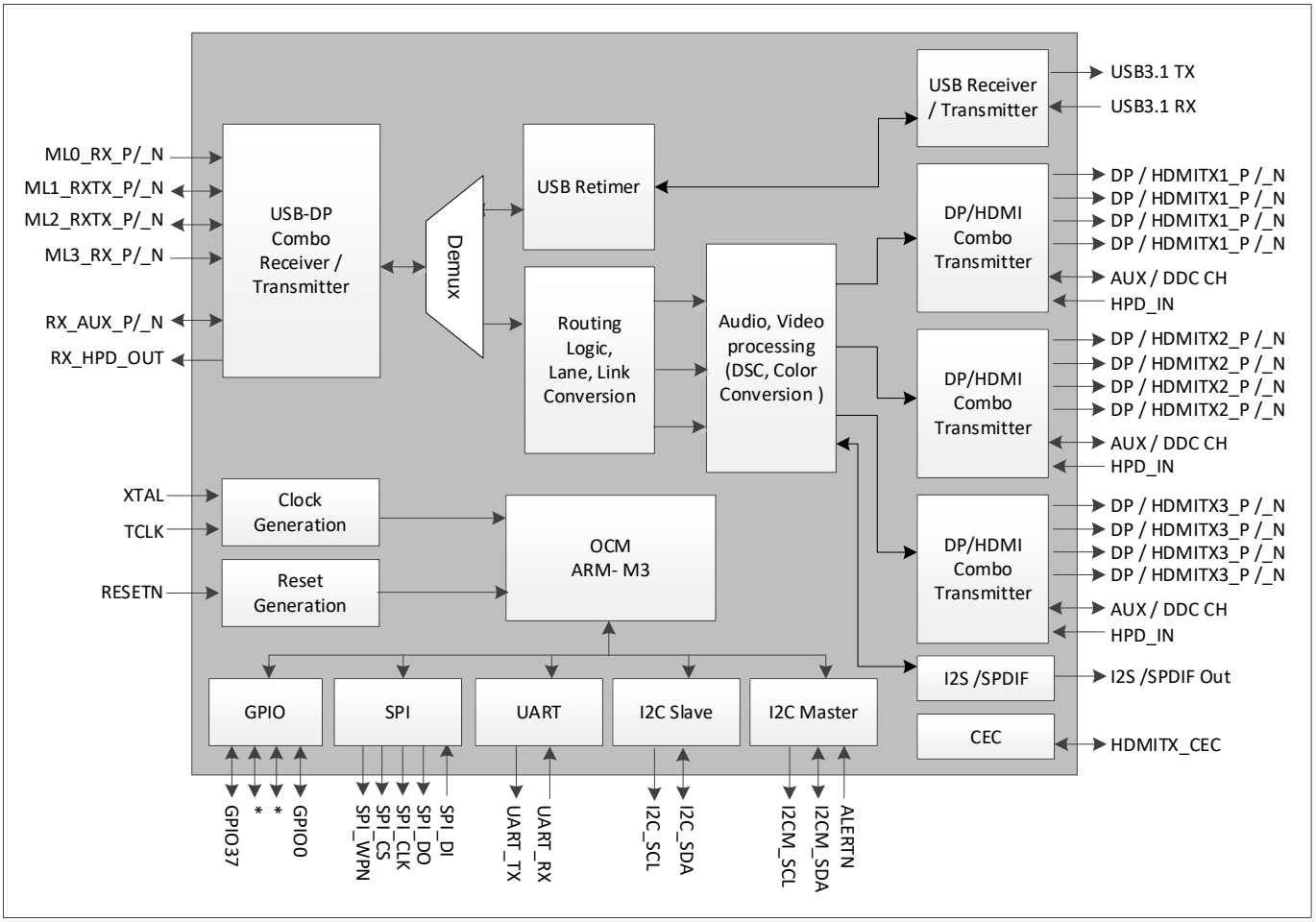


Figure 3. KTM5030 AR/VR Head Mount Display Use Case

Functional Block Diagram



BGA Footprints and Pin Mapping

The ball grid array (BGA) diagrams give the allocation of pins to the package shown, from the top looking down, using the PCB footprint.

Some signal names in BGA diagrams have been abbreviated. Refer to the pin list for full signal names sorted by pin number.

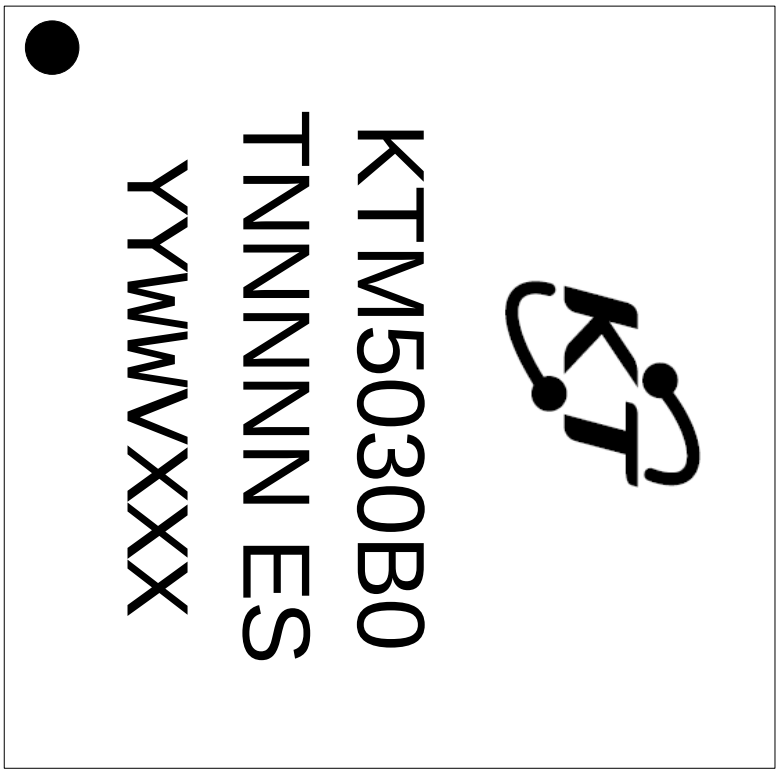
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	
A	HPD_OUT_GPIO2	GND	SSRX2P_RX3N	GND	SSTX2P_RX2N	GND	RX_REXT	REFCLK_OUT	GND	SSTX1P_RX1P	GND	SSRX1P_RX0P	GND	TX0_SSRXP	GND	TX0_SSTXP	GND	A
B	I2CM_SCL_PCONF1	GND	SSRX2N_RX3P	GND	SSTX2N_RX2P	GND	EXT_RESETN	GND	GND	SSTX1N_RX1N	GND	SSRX1N_RX0N	GND	TX0_SSRXN	GND	TX0_SSTXN	GND	B
C	ALERTN_PPOL	GND	GND	GND	GND	GND	XTAL_IN	XTAL_OUT	GND	AVDD18_UFP	AVDD18_UFP	AVDD18_UFP	AVDD18_UFP	GND	GND	GND	GND	C
D	I2CM_SDA_PCONF0	GND	RX_AUXN_SBU1	RX_AUXP_SBU2	AVDDP9_UFP	AVDDP9_UFP	AVDDP9_UFP	AVDDP9_UFP	AVDDP9_UFP	AVDDP9_UFP	AVDDP9_UFP	AVDDP9_UFP	AVDDP9_UFP	GND	NC	TX1_CONFIG1_GPIO11	SPI_DO	D
E	TX3_DDC_SCL	GPIO0_I2C_SDA	GND	DVDDP9	GND	GND	GND	GND	GND	GND	GND	GND	GND	DVDDP9	DVDD18	SPI_CLK	SPI_HOLD	E
F	TX3_HPD_IN	GPIO1_I2C_SCL	GND	DVDDP9	GND	GND	GND	GND	GND	GND	GND	GND	GND	DVDDP9	DVDD18	SPI_CSN	SPI_DI	F
G	TX2_DDC_SCL	TX3_DDC_SDA	DVDD18	DVDDP9	GND	GND	GND	GND	GND	GND	GND	GND	GND	DVDDP9	TEST	SPI_WPN	URX_GPIO8	G
H	TX1_DDC_SDA	TX2_DDC_SDA	DVDD18	DVDDP9	GND	GND	GND	GND	GND	GND	GND	GND	GND	DVDDP9	DVDD18	UTX_GPIO9	TX2_CONFIG1_GPIO12	H
J	TX1_DDC_SCL	TX2_HPD_IN	GND	DVDDP9	GND	GND	GND	GND	GND	GND	GND	GND	GND	DVDDP9	DVDD18	DBUG0_GPIO6	TX3_CONFIG1_GPIO13	J
K	TX1_CEC_GPIO10	TX1_HPD_IN	GND	DVDDP9	GND	GND	GND	GND	GND	GND	GND	GND	GND	DVDDP9	DVDD18	I2S_WCK_GPIO14	DBUG1_GPIO7	K
L	TX3_CEC_GPIO36	GPIO37_TX2_CEC	GND	DVDDP9	GND	GND	GND	GND	GND	GND	GND	GND	GND	DVDDP9	DVDD18	I2S_D0_GPIO16	I2S_FCK_GPIO15	L
M	GND	GND	TX2_AUX_N	DVDDP9	GND	GND	GND	GND	GND	GND	GND	GND	GND	DVDDP9	I2S_D2_GPIO18	I2S_D3_GPIO19	I2S_D1_GPIO17	M
N	TX1_L3_HDMICLK_N	GND	TX2_AUX_P	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	GND	N
P	TX1_L3_HDMICLK_P	GND	TX1_AUX_N	AVDDP9_TX	AVDDP9_TX	AVDDP9_TX	AVDDP9_TX	AVDDP9_TX	AVDDP9_TX	AVDDP9_TX	AVDDP9_TX	AVDDP9_TX	AVDDP9_TX	GND	TX3_AUX_N	GND	TX3_L0_HDMICH2_P	P
R	TX1_L2_HDMICH0_N	GND	TX1_AUX_P	AVDD18_TX	TX1_CM	AVDD18_TX	AVDD18_TX	TX2_CM	AVDD18_TX	AVDD18_TX	AVDD18_TX	TX3_CM	AVDD18_TX	GND	TX3_AUX_P	GND	TX3_L0_HDMICH2_N	R
T	TX1_L2_HDMICH0_P	GND	GND	GND	GND	TX2_L3_HDMICLK_N	GND	GND	GND	GND	TX2_L0_HDMICH2_P	GND	GND	GND	GND	GND	TX3_L1_HDMICH1_P	T
U	TX1_L1_HDMICH1_N	TX1_L1_HDMICH1_P	TX1_L0_HDMICH2_N	TX1_L0_HDMICH2_P	GND	TX2_L3_HDMICLK_P	TX2_L2_HDMICH0_N	TX2_L2_HDMICH0_P	TX2_L1_HDMICH1_N	TX2_L1_HDMICH1_P	TX2_L0_HDMICH2_N	GND	TX3_L3_HDMICLK_N	TX3_L3_HDMICLK_P	TX3_L2_HDMICH0_N	TX3_L2_HDMICH0_P	TX3_L1_HDMICH1_N	U
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	

TOP VIEW

10GHz SERDES	GND	ANALOG	DIGITAL 1.8V I/O	DIGITAL 5V TOL OPEN-DRAIN I/O	0.9V DIGITAL	0.9V ANALOG	1.8V DIGITAL	1.8V ANALOG VDD

289-Pin 12.0mm x 12.0mm x 1.3mm
LFBGA Package, 0.65mm pitch

Figure 4. KTM5030 BGA Diagram



289-Pin 12.0mm x 12.0mm x 1.3mm
LFBGA Package, 0.65mm pitch

Table 2. Field Marking Description

Field	Description	Marking
DOT	Pin1 indicator	DOT
Line 1	Company logo	Kinetic Logo
Line 2	Part Number + IC revision	KTM5030B0
Line 3	Traceability codes TNNNNN: Fab Lot Number ES: for Engineering Samples	"Variant"
Line 4	YYWW: Assembly Date Code (Work Year & Work Week) V: Assembly Vendor Code XXX: Serial Number	"Variant"

Table 3. Pin List

Pin #	Name	Pin #	Name	Pin #	Name
A1	HPD_OUT_GPIO2	C9	GND	E17	SPI_HOLD
A2	GND	C10	AVDD18_UFP	F1	TX3_HPD_IN
A3	SSRX2P _RX3N	C11	AVDD18_UFP	F2	GPIO1_I2C_SCL
A4	GND	C12	AVDD18_UFP	F3	GND
A5	SSTX2P _RX2N	C13	AVDD18_UFP	F4	DVDDP9
A6	GND	C14	GND	F5	GND
A7	RX_REXT	C15	GND	F6	GND
A8	REFCLK_OUT	C16	GND	F7	GND
A9	GND	C17	GND	F8	GND
A10	SSTX1P _RX1P	D1	I2CM_SDA_PCONF0	F9	GND
A11	GND	D2	GND	F10	GND
A12	SSRX1P _RX0P	D3	RX_AUXN_SBU1	F11	GND
A13	GND	D4	RX_AUXP_SBU2	F12	GND
A14	TX0_ SSRXP	D5	AVDDP9_UFP	F13	GND
A15	GND	D6	AVDDP9_UFP	F14	DVDDP9
A16	TX0_ SSTXP	D7	AVDDP9_UFP	F15	DVDD18
A17	GND	D8	AVDDP9_UFP	F16	SPI_CSN
B1	I2CM_SCL_PCONF1	D9	AVDDP9_UFP	F17	SPI_DI
B2	GND	D10	AVDDP9_UFP	G1	TX2_DDC_SCL
B3	SSRX2N _RX3P	D11	AVDDP9_UFP	G2	TX3_DDC_SDA
B4	GND	D12	AVDDP9_UFP	G3	DVDD18
B5	SSTX2N _RX2P	D13	AVDDP9_UFP	G4	DVDDP9
B6	GND	D14	GND	G5	GND
B7	EXT_RESETN	D15	NC	G6	GND
B8	GND	D16	TX1_ CONFIG1_GPIO11	G7	GND
B9	GND	D17	SPI_DO	G8	GND
B10	SSTX1N _RX1N	E1	TX3_DDC_SCL	G9	GND
B11	GND	E2	GPIO0_I2C_SDA	G10	GND
B12	SSRX1N _RX0N	E3	GND	G11	GND
B13	GND	E4	DVDDP9	G12	GND
B14	TX0_ SSRXN	E5	GND	G13	GND
B15	GND	E6	GND	G14	DVDDP9
B16	TX0_ SSTXN	E7	GND	G15	TEST
B17	GND	E8	GND	G16	SPI_WPN
C1	ALERTN_PPOL	E9	GND	G17	URX_GPIO8
C2	GND	E10	GND	H1	TX1_DDC_SDA
C3	GND	E11	GND	H2	TX2_DDC_SDA
C4	GND	E12	GND	H3	DVDD18
C5	GND	E13	GND	H4	DVDDP9
C6	GND	E14	DVDDP9	H5	GND
C7	XTAL_IN	E15	DVDD18	H6	GND
C8	XTAL_OUT	E16	SPI_CLK	H7	GND

Continues on page 12

Pint List (Continued)

Pin #	Name
H8	GND
H9	GND
H10	GND
H11	GND
H12	GND
H13	GND
H14	DVDDP9
H15	DVDD18
H16	UTX_GPIO9
H17	TX2_ CONFIG1_GPIO12
J1	TX1_DDC_SCL
J2	TX2_HPD_IN
J3	GND
J4	DVDDP9
J5	GND
J6	GND
J7	GND
J8	GND
J9	GND
J10	GND
J11	GND
J12	GND
J13	GND
J14	DVDDP9
J15	DVDD18
J16	DBUG0_GPIO6
J17	TX3_ CONFIG1_GPIO13
K1	TX1_CEC_GPIO10
K2	TX1_HPD_IN
K3	GND
K4	DVDDP9
K5	GND
K6	GND
K7	GND
K8	GND
K9	GND
K10	GND
K11	GND
K12	GND
K13	GND
K14	DVDDP9
K15	DVDD18

Pin #	Name
K16	I2S_WCK_GPIO14
K17	DBUG1_GPIO7
L1	TX3_CEC_GPIO36
L2	GPIO37_TX2_CEC
L3	GND
L4	DVDDP9
L5	GND
L6	GND
L7	GND
L8	GND
L9	GND
L10	GND
L11	GND
L12	GND
L13	GND
L14	DVDDP9
L15	DVDD18
L16	I2S_D0_GPIO16
L17	I2S_FCK_GPIO15
M1	GND
M2	GND
M3	TX2_AUX_N
M4	DVDDP9
M5	GND
M6	GND
M7	GND
M8	GND
M9	GND
M10	GND
M11	GND
M12	GND
M13	GND
M14	DVDDP9
M15	I2S_D2_GPIO18
M16	I2S_D3_GPIO19
M17	I2S_D1_GPIO17
N1	TX1_L3_HDMICLK_N
N2	GND
N3	TX2_AUX_P
N4	GND
N5	GND
N6	GND

Pin #	Name
N7	GND
N8	GND
N9	GND
N10	GND
N11	GND
N12	GND
N13	GND
N14	GND
N15	GND
N16	GND
N17	GND
P1	TX1_L3_HDMICLK_P
P2	GND
P3	TX1_AUX_N
P4	AVDDP9_TX
P5	AVDDP9_TX
P6	AVDDP9_TX
P7	AVDDP9_TX
P8	AVDDP9_TX
P9	AVDDP9_TX
P10	AVDDP9_TX
P11	AVDDP9_TX
P12	AVDDP9_TX
P13	AVDDP9_TX
P14	GND
P15	TX3_AUX_N
P16	GND
P17	TX3_L0_HDMICH2_P
R1	TX1_L2_HDMICH0_N
R2	GND
R3	TX1_AUX_P
R4	AVDD18_TX
R5	TX1_CM
R6	AVDD18_TX
R7	AVDD18_TX
R8	TX2_CM
R9	AVDD18_TX
R10	AVDD18_TX
R11	AVDD18_TX
R12	TX3_CM
R13	AVDD18_TX
R14	GND

Continues on page 13

Pint List (Continued)

Pin #	Name
R15	TX3_AUX_P
R16	GND
R17	TX3_L0_HDMICH2_N
T1	TX1_L2_HDMICH0_P
T2	GND
T3	GND
T4	GND
T5	GND
T6	TX2_L3_HDMICLK_N
T7	GND
T8	GND
T9	GND
T10	GND
T11	TX2_L0_HDMICH2_P
T12	GND
T13	GND
T14	GND
T15	GND
T16	GND
T17	TX3_L1_HDMICH1_P
U1	TX1_L1_HDMICH1_N
U2	TX1_L1_HDMICH1_P
U3	TX1_L0_HDMICH2_N
U4	TX1_L0_HDMICH2_P
U5	GND
U6	TX2_L3_HDMICLK_P
U7	TX2_L2_HDMICH0_N
U8	TX2_L2_HDMICH0_P
U9	TX2_L1_HDMICH1_N
U10	TX2_L1_HDMICH1_P
U11	TX2_L0_HDMICH2_N
U12	GND
U13	TX3_L3_HDMICLK_N
U14	TX3_L3_HDMICLK_P
U15	TX3_L2_HDMICH0_N
U16	TX3_L2_HDMICH0_P
U17	TX3_L1_HDMICH1_N

Ordering Information

Part Number	Functional Description	Marking[1]	Operating Temperature	Package	External Package
KTM5030B0	USB-C/ DP alt-mode DP 4 lanes OR 2 lanes DP and 2 lanes USB3.2 DSC	KTM5030B0	0°C to +70°C	289- LFBGA	TRAYS
KTM5030B0T					Tape and Reel

Absolute Maximum Ratings[2]

(T_A = 25°C unless otherwise noted)

Symbol	Description	Value	Units
$V_{VDD\_1.8}$	VDD1.8V to GND	-0.3 to 2.16	V
$V_{VDD\_0.95}$	VIO0.95V to GND	-0.3 to 1.14	V
V_{IN5tol}	Input voltage tolerance for 3.3V, 5V tolerant I/O pins	-0.3 to 5.5	V
T_{STG}	Storage temperature	-40 to 150	°C
T_{SOL}	Peak IR reflow soldering temperature	260	°C

ESD and Latch-up Ratings[3]

Symbol	Description	Value	Units
V_{ESD_HBM}	JEDEC JESD22-A114 ESD HBM (all pins)	±2.0	kV
V_{ESD_CDM}	JEDEC JESD22-C101 ESD CDM (all pins)	±500	V
I_{LU}	JEDEC JESD78	±100	mA

Thermal Capabilities[4]

Symbol	Description	Value	Units
Θ_{JA}	Thermal Resistance – Junction to Ambient	27	°C/W
Θ_{JC}	Thermal Resistance – Junction to Case	8.473	°C/W
T_A	Ambient Operating Temperature Range	0 to 70	°C
T_J	Junction Operating Temperature Range	0 to 125	°C

1. See Table 1 for trace codes marking details;. ES – Engineering Sample.
2. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
3. ESD and Latch-up Ratings conform to JEDEC industry standards. Some pins may actually have higher performance. Ratings apply with chip enabled, disabled, or unpowered, unless otherwise noted.
4. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to a four-layer JEDEC PCB board, no heat spreader, and no air flow.

Electrical Characteristics[5]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of 0°C to +70°C and $V_{DD\_1.8V}$ = 1.8V, $V_{DD\_0.95V}$ = 0.95V. Typical values are specified at T_A = +25°C.

DC Characteristics

Supply Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{VDD\_1.8}$	1.8V supply voltages (analog and digital)		1.71	1.8	1.89	V
$V_{VDD\_0.9}$	0.95V supply voltages (analog and digital)		0.90	0.95	1.00	V
Power						
	Protocol converter Mode Measurement condition: Nominal corner, 25°C, Nominal power supply					
	Operating condition 1 Input: DP MST HBR3 (4L) Output1: DP SST HBR3 (4L) 4k2k30Hz Output2: DP SST HBR3 (4L) 4k2k30Hz Output3: HDMI 4k2k30Hz			550	600	mW
	Operating condition 2 Input: DP MST HBR3 (4L) Output1: DP SST HBR3 (4L) 1080p60Hz Output2: DP SST HBR3 (4L) 4k2k30Hz Output3: HDMI 4k2k60Hz			626	711	mW
	Operating condition 3 Input: DP SST HBR3 (4L) 4k2k60Hz Output1: DP SST HBR3 (4L) 4k2k60Hz Output2: DP SST HBR3 (4L) 4k2k60Hz Output3: HDMI 4k2k60Hz			712	795	mW
	Standby			9.2		mW
$I_{DD\_0.95V}$	0.95V Supply Current	Nominal corner, 25°C, Nominal power supply Operating condition 3 (See above) VDD (analog and digital) 0.95V VDD (analog and digital) 1.8V		733[6]	892	mA
$I_{DD\_1.8V}$	1.8V Supply Current[7]			146	155	mA
T_{RAMP_MIN}	Minimum Power Rail Ramp up Time		100			µS

5. Device is guaranteed to meet performance specifications over the 0°C to +70°C operating temperature range by design, characterization and correlation with statistical process controls.

6. Values are for Power Supply design only and not indicative for Max Power Consumption.

7. Ripple amplitude for power supplies should be 20mV or lower with max ripple frequency up to 30MHz.

Electrical Characteristics[5] (continued)

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of 0°C to +70°C and $V_{DD\_1.8V}$ = 1.8V, $V_{DD\_0.95V}$ = 0.95V. Typical values are specified at T_A = +25°C.

3.3V IO Signals, 5V Tolerant Open Drain Type

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{PAD}	Input Voltage at PAD			5	6	V
V_{IH}	Input High voltage		2.0			V
V_{IL}	Input Low voltage				0.8	V
V_{OL}	Output Low voltage				0.4	V
I_{OL}	Output Low current (measured at V_{OL} = 0.4V)		5.3	8.7	10.7	mA
I_{IL}	Input Leakage current			2.4	3.8	µA
I_{IL_off}	Input Leakage in Fail Safe (unpowered VDD/VREF)			2	3.2	µA
I_{vref}	VREF DC current			0.1	0.8	nA
I_{vdd}	VDD DC current			0.8	3.9	µA

1.8V IO Signals, 1.8V Tolerant, TRISTATE

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{IH}	Input High voltage		1.25			V
V_{IL}	Input Low voltage				0.55	V
V_{OL}	Output Low voltage				0.45	V
V_{OH}	Output High voltage		1.35			V
I_{IH}	Input Leakage current		-10		10	µA
I_{IL}			-10		10	µA
I_{OZ}	Tri-state output Leakage current		-10		10	µA
R_{PU}	Pull-up Resistor			80		kΩ
R_{PD}	Pull-down Resistor			95		kΩ

Electrical Characteristics[5] (continued)

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of 0°C to +70°C and $V_{DD\_1.8V}$ = 1.8V, $V_{DD\_0.95V}$ = 0.95V. Typical values are specified at T_A = +25°C.

AC Characteristics[8]

Maximum Speed of Operation

Symbol	Description	Conditions	Min	Typ	Max	Units
T_{CLK}	Reference Input Clock				25	MHz
O_{CLK}	On-Chip Microcontroller Clock				300	MHz
$SLAVE_{\_SCL}$	I2C host interface clock				400	kHz
$MSTRx_{\_SCL}$	DDC Master				400	kHz
SPI	SPI Clock				75	MHz

DisplayPort Receiver Characteristics

Receiver Operating Range

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{RX\_DIF\_PP\_RANGE}$	Differential Input Voltage Range		40		800	mV
$R_{RX\_TERM\_RANGE}$	RX Termination Control Range		80	100	120	Ω

System Parameters

Symbol	Description	Conditions	Min	Typ	Max	Units
UI_{HBR3}	HBR3 unit interval (8.1Gbps)			123		Ps
UI_{HBR2}	HBR2 unit interval (5.4Gbps)			185		Ps
UI_{HBR}	HBR unit interval (2.7Gbps)			370		Ps
UI_{RBR}	RBR unit interval (1.62Gbps)			617		ps
	Link clock down spreading	Modulation frequency range of 30kHz to 33kHz	0		0.5	%

8. AC characteristics parameters are guaranteed by the silicon characterization across operating condition unless otherwise specified. Not all parameters are tested in the production test.

Electrical Characteristics[5] (continued)

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of 0°C to +70°C and $V_{DD\_1.8V}$ = 1.8V, $V_{DD\_0.95V}$ = 0.95V. Typical values are specified at T_A = +25°C.

Main Link and AUX CH Parameters

Symbol	Description	Conditions	Min	Typ	Max	Units
Main Link Jitter Tolerance, Target Bit Error Rate 10^{-9}						
$T_{RX\_TJ\_RBR}$	RBR Total jitter at TP3	EH = 56 mVdiff_pp			0.747	UI
$T_{RX\_Non-ISI\_RBR}$	RBR non-ISI jitter				0.177	UI
$T_{RX\_TJ\_HBR}$	HBR Total jitter at TP3_EQ	EH = 160 mVdiff_pp			0.491	UI
$T_{RX\_Non-ISI\_HBR}$	HBR non-ISI jitter				0.330	UI
$T_{RX\_TJ\_HBR2}$	HBR2 Total jitter at TP3_EQ	EH = 100 mVdiff_pp			0.62	UI
$T_{RX\_Non-ISI\_HBR2}$	HBR2 non-ISI jitter				0.40	UI
$T_{RX\_TJ\_HBR3}$	HBR3 Total jitter at TP3_CTLE	EH = 50 mVdiff_pp			0.62	UI
$T_{RX\_NON\_ISI\_HBR3}$	HBR3 non-ISI jitter				0.38	UI
AUX Parameters						
$V_{AUX\_RX\_DIF\_RANGE}$	Differential Input Voltage Range	TP3	0.27		1.36	V
$V_{AUX\_TX\_DIF\_RANGE}$	Differential Output Voltage Range		0.29		1.38	V
$R_{AUX\_TERM\_RANGE}$	RX DIFF Termination Control Range			100		Ω

Electrical Characteristics[5] (continued)

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of 0°C to +70°C and $V_{DD\_1.8V}$ = 1.8V, $V_{DD\_0.95V}$ = 0.95V. Typical values are specified at T_A = +25°C.

DisplayPort Transmitter Characteristics

Transmitter Operating Range

Symbol	Description	Conditions	Min	Typ	Max	Units
$V_{TX\_DIF\_PP\_RANGE}$	Differential Output Voltage Range				1.38	V
$R_{TX\_TERM\_RANGE}$	TX Termination Control Range		80	100	120	Ω
DisplayPort Transmitter System Parameters						
UI_{HBR3}	HBR3 unit interval (8.1Gbps)			123		ps
UI_{HBR2}	HBR2 unit interval (5.4Gbps)			185		ps
UI_{RBR}	HBR unit interval (2.7Gbps)			370		ps
UI_{RBR}	RBR unit interval (1.62Gbps)			617		ps
	Link clock down spreading	Modulation frequency range of 30kHz to 33kHz	0		0.5	%
C_{TX}	Coupling capacitor	All Main lanes and AUX CH need AC coupling on the transmitter side		100		nF
DisplayPort Transmitter TP2 Parameters						
$T_{TX\_SKEW\_INTER\_PAIR}$	Lane-to-Lane output Skew	Applies to all pairwise combinations of supported lanes			1250	ps
$T_{TX\_SKEW\_INRA\_PAIR}$	Lane Intra pair Skew	Applies to all supported lanes			30	ps
Target bit error rate 10^{-9}						
$T_{TX\_TJ\_TPS4\_HBR3}$	HBR3 Total Jitter at TP3_CTLE	VSL/PEL = 1/1, A_{dc} = -3 dB			0.47	UI
$T_{TX\_NonISI\_TPS4\_HBR3}$	HBR3 Non-ISI Jitter				0.23	UI
$T_{TX\_TJ\_CP2520\_HBR2}$	HBR2 Total Jitter at TP3_EQ	VSL/PEL = 1/1			0.58	UI
$T_{TX\_NonISI\_CP2520\_HBR2}$	HBR2 Non-ISI Jitter				0.36	UI
$T_{TX\_TJ\_D10.2\_HBR2}$	HBR2 Total Jitter with D10.2	Measured at TP3_EQ			0.40	UI
$T_{TX\_DJ\_D10.2\_HBR2}$	HBR2 Dual-Dirac Jitter with D10.2	Measured at TP3_EQ			0.27	UI
$T_{TX\_RJ\_D10.2\_HBR2}$	HBR2 Random Jitter with D10.2	Measured at TP3_EQ			19.2	mUIrms
AUX Parameters						
$V_{AUX\_RX\_DIFF\_PP}$	Differential Input Voltage Range		0.27		1.38	V
$V_{AUX\_TX\_DIFF\_PP}$	Differential Output Voltage Range	50mV/step in 4 steps	0.29		1.38	V
$R_{AUX\_TERM\_RANGE}$	RX DIFF Termination Control Range			100		Ω

Electrical Characteristics[5] (continued)

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of 0°C to +70°C and $V_{DD\_1.8V}$ = 1.8V, $V_{DD\_0.95V}$ = 0.95V. Typical values are specified at T_A = +25°C.

HDMI Transmitter I/O Characteristics

HDMI Transmitter DC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
V_{TX_PP}	Differential output: single ended swing amplitude		0.4	0.5	0.6	V
$V_{TX\_DIF\_HIGH}$	Differential output: Single ended high-level output	Sink supply dependent (typical V_{DD} = 3.3V)		3.3		V

HDMI Transmitter AC Specifications

Symbol	Description	Conditions	Min	Typ	Max	Units
$f_{TX\_CHR\_CLK}$	TMDS Character Clock	Programmable	25		600	MHz
$V_{TX\_DIF\_PP}$	Differential Output Voltage	In 64 steps (usable range 0.8 – 1.2 V)	0		1.2	V
A_{PREMPH}	TX Pre-Emphasis Level	$V_{TX\_DIF\_PP}$ + A_{PREMPH} should be less than 1.2 V	0		6	dB
$R_{TX\_TERM\_RANGE}$	TX Differential Termination Control Range	Programmable Termination (range 85-600)		100		Ω
$T_{TX\_CLK\_JITTER}$	TX Clock jitter	Tighter than HDMI specification			0.25	TBIT
	TX Data Jitter	Refer to the tables below.				

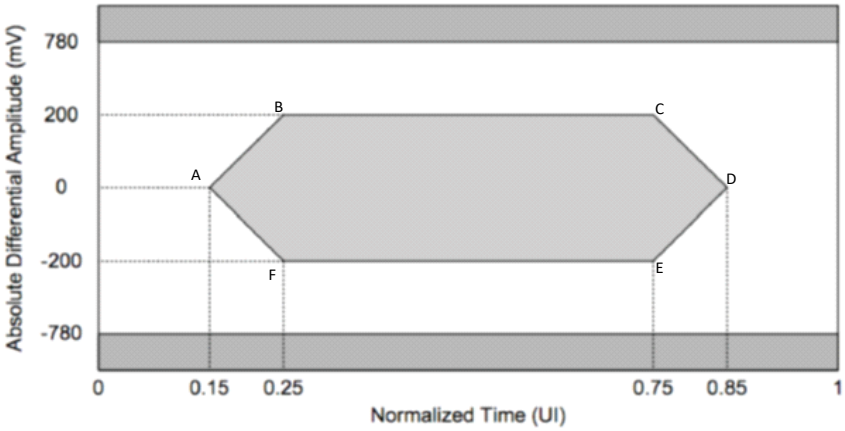


Figure 5. HDMI1.4b EYE Diagram at TP1 at TMDS Character Clock Rate ≤ 340MHz

Table 4. TMDS TX EYE Opening Specification for TMDS Character Clock Rate ≤ 340MHz

Point	H(UI)	V (mV_diff_pp)
A	0.13	0
B	0.20	200
C	0.80	200
D	0.87	0
E	0.80	-200
F	0.20	-200

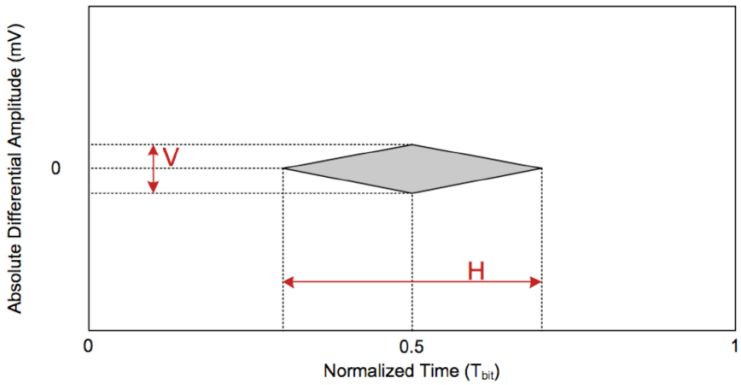


Figure 6. HDMI2.0 EYE Diagram at TP2_EQ at TMDS Character Clock Rate > 340MHz

Table 5. TMDS TX PHY Jitter Specification at TMDS Character Clock Rate > 340 MHz

TMDS Bit Rate (Gbps)	H (Tbit)	V (mV_diff_pp)
3.4 < Rbit < 3.712	0.72	335
3.712 < Rbit ≤ 5.94	-0.0332 $Rbit^2$ + 0.2312 Rbit + 0.1998	-19.66 $Rbit^2$ + 106.74 Rbit + 209.58
5.94 < Rbit ≤ 6.0	0.48	150

USB 3.2x1 Transmitter and Receiver Characteristics

USB 3.2 x1 transmitter (SSRX pin and Type-C interface in USB mode)

Symbol	Description	Conditions	Min	Typ	Max	Units
UI_{USB_GEN1}	Unit interval in Gen1		199.94		200.46	ps
UI_{USB_GEN2}	Unit interval in Gen2		99.97		100.03	ps
C_{TX_USB}	AC coupling capacitor		75		265	nF
$t_{SSC\_FREQ\_DEVIATION}$	SSC deviation		0		-5000	ppm
$t_{SSC\_MOD\_RATE}$	Modulation rate		30		33	kHz
$V_{USB\_TX\_DIFF\_PP}$	Differential peak-to-peak voltage swing		0.8		1.2	V
$V_{TX\_DE\_RATIO\_GEN1}$	De-emphasis in Gen1		3.0		4.0	dB
$V_{TX\_PS\_RATIO}$	Pre-shoot in Gen2		1.2		3.2	dB
$V_{TX\_DE\_RATIO\_GEN2}$	De-emphasis in Gen2		2.1		4.1	dB
$R_{TX\_DIFF\_DC}$	DC differential impedance		72		120	Ω
$V_{TX\_RCV\_DETECT}$	The amount of voltage change during Rx detection				0.6	V
$t_{CDR\_SLEW\_RATE}$	Maximum slew rate	In Gen1			10	ms/s
SSC_{dfdt}	SSC df/dt	In Gen2			1250	ppm/µs
$V_{EYE\_HEIGHT\_GEN1}$	Eye height at TP4 in Gen1		100		1000	mV
$V_{EYE\_HEIGHT\_GEN2}$	Eye height at TP4 in Gen2		70		1000	mV
Dj_{USB_GEN1}	Deterministic jitter at TP4 in Gen1				430	mUI
Dj_{USB_GEN2}	Deterministic jitter at TP4 in Gen2				530	mUI
Rj_{USB_GEN1}	RMS Random jitter at TP4 in Gen1				3.22	ps
Dj_{USB_GEN2}	RMS Deterministic jitter at TP4 in Gen2				1	ps
Tj_{USB_GEN1}	Total jitter at TP4 in Gen1				660	mUI
Tj_{USB_GEN1}	Total jitter at TP4 in Gen2				671	mUI
t_{PERIOD}	LFPS t_{PERIOD}		20		80	ns
$V_{TX\_DIFF\_PP\_LFPS}$	LFPS peak-to-peak differential amplitude		800		1000	mV
T_{DUTY_LFPS}	LFPS duty cycle		40		60	%

USB 3.2 x1 Receiver (SSRX pin and Type-C interface in USB mode)

Symbol	Description	Conditions	Min	Typ	Max	Units
UI_{USB_GEN1}	Unit interval in Gen1		199.94		200.46	ps
UI_{USB_GEN2}	Unit interval in Gen2		99.97		100.23	ps
$t_{SSC\_FREQ\_DEVIATION}$	SSC deviation		0		-5000	ppm
$t_{SSC\_MOD\_RATE}$	Modulation rate		30		33	kHz
R_{RX_DC}	Receiver DC common mode impedance		18		30	Ω
$R_{RX\_DIFF\_DC}$	DC differential impedance		72		120	Ω
$Z_{RX\_HIGH\_IMP\_DC\_POS}$	Receiver high impedance		10k			Ω
$V_{RX\_LFPS\_DET\_DIFFp-p}$	LFPS detect threshold		100		300	mV

DDC (I2C) Interface Timing Characteristics

DDC (I2C) Interface Timing

Symbol	Description	Conditions	Min	Typ	Max	Units
f_{SCL}	SCL clock rate	Fast mode	0	-	400	kHz
t_{HD-STA}	Hold time START	After this period, the 1st clock starts	1.2	-	-	µs
t_{LOW}	Low period of clock	SCL	1.3	-	-	µs
t_{HIGH}	High period of clock	SCL	1.2	-	-	µs
$t_{su;STA}$	Set up time for a repeated START		1.2	-	-	µs
$t_{HD;DAT}$	Data hold time	For master	0.7	-	0.9[9]	µs
$t_{SU;DAT}$	Data setup time		380	-	-	ns
T_{BUF}	Bus free time between STOP and START		1.3	-	-	µs
C_B	Capacitance load for each bus line		-	100	400	pF
t_r	Rise time		220	-	300	ns
t_f	Fall time		60	-	300	ns
V_{nh}	Noise margin at high level		0.25 VDD	-	-	V
V_{nl}	Noise margin at low level		0.2 VDD	-	-	V

9. The maximum $t_{HD;DAT}$ only has to be met if the device does not stretch the low period t_{LOW} of the SCL signal. In the diagram below, S = start, P = stop, Sr = Repeated start, and SP = Repeated stop conditions.

I2C Host Interface Timing (Figure 7. I2C Timing)

Symbol	Description	Min	Typ	Max	Units
F_{SCL}	SCL Clock Frequency			400	kHz
$t_{hd: DAT}$	Data hold time	0		-	µs
$t_{SU :DAT}$	Data set-up time	50		-	ns
t_R	Rise time of both SDA and SCL signals	-		120	ns
t_F	Fall time of both SDA and SCL signals	20x (V_{DD}/5.5)		120	ns
t_{BUF}	Bus free time between a STOP and START condition	0.5		-	µs
C_B	Capacitance load for each bus line	-		550	pF
$t_{VD: DAT}$	Data valid time	-		0.45	µs
$t_{VD: ACK}$	Data valid acknowledge time	-		0.45	µs
t_{I2C_SBR} (400 kHz)	Time for I2C SINGLE BYTE READ	-		110	µs
t_{I2C_SBW} (400 kHz)	Time for I2C SINGLE BYTE WRITE	-		85	µs
t_{I2C_MBR} (400 kHz)	Time for I2C Multi BYTE READ	-		100+35/byte	µs
t_{I2C_MBW} (400 kHz)	Time for I2C Multi BYTE WRITE			85+30/byte	µs

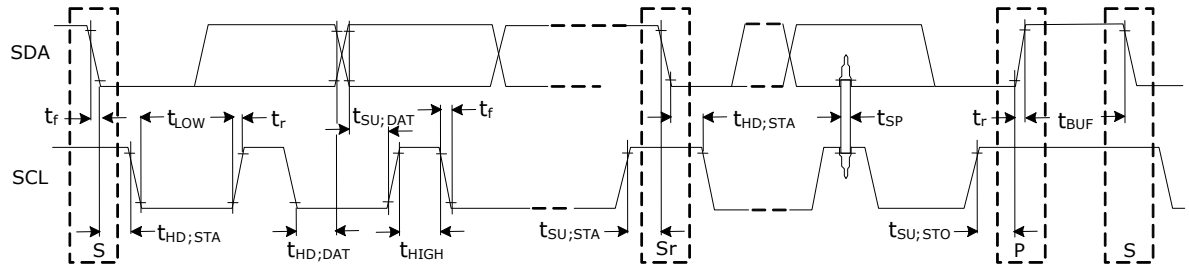


Figure 7. I2C Timing

SPI Interface Timing Characteristics

SPI Interface Timing for Normal Operating Mode[10]

Symbol	Description	Min	Typ	Max	Units
F_{CLK}	SPI_CLK output clock frequency for normal SPI mode		50	75	MHz
T_{SCKH}	Serial clock high time	9.2			ns
T_{SCKL}	Serial clock low time	9.2			ns
$T_{R\_SPI\_CLK}$	SPI_CLK rise time @10mA drive 10pF load			2.8	ns
$T_{F\_SPI\_CLK}$	SPI_CLK fall time @10mA drive 10pF load			3.2	ns
T_{CSN_SU}	CSN output setup time requirement	7			ns
T_{CSN_HLD}	CSN output hold time requirement	7			ns
$T_{\_DO\_PD}$	Data Output propagation delay			6	ns
T_{DI_SU}	Data Input setup time	3			ns
T_{DI_HLD}	Data Input hold time	5			ns

10. These specifications specify the typical SPI_CLK output frequency and the minimum requirements of the interface between the SPI NOR Flash device and KTM5030.

Interface Description

UFP AV Interface

The UFP AV interface consists of 4 highspeed lanes, Auxiliary channel (Side band channel) and HPD out. The high-speed lanes can receive DP audio-video streams or USB data from a source device through DP or USB Type-C link. The high-speed lane mapping is configurable to match the standard DP connector or the USB Type-C connector. The following table shows the KTM5030 high-speed main lanes and side band channel signal mapping for the USB Type-C and DP connector.

USB TYPE-C CONNECTOR		STRAIGHT MAP		FLIPPED MAP		STD DP CONNECTOR		KTM5030		
		Assignment C	Assignment D	Assignment C	Assignment D					
PIN	NAME	DP	DP + USB	DP_BR	DP_BR+USB	PIN	NAME	PIN	SIGNAL NAME	RX PHY
B8	SBU2	AUX_CH_P	AUX_CH_P	AUX_CH_N	AUX_CH_N	15	AUX_CH_P	D4	RX_AUXP_SBU2	AUX CH
A8	SBU1	AUX_CH_N	AUX_CH_N	AUX_CH_P	AUX_CH_P	17	AUX_CH_N	D3	RX_AUXN_SBU1	
B11	RX1+	ML2+	SSRX+	ML1+	ML1+	12	ML0_P	A12	RX_L0P_SSRX1P	LANE 0
B10	RX1-	ML2-	SSRX-	ML1-	ML1-	10	ML0_N	B12	RX_L0N_SSRX1N	
A2	TX1+	ML3+	SSTX+	ML0+	ML0+	9	ML1_P	A10	RX_L1P_SSTX1P	LANE1
A3	TX1-	ML3-	SSTX-	ML0-	ML0-	7	ML1_N	B10	RX_L1N_SSTX1N	
B3	TX2-	ML0-	ML0-	ML3-	SSTX-	6	ML2_P	B5	RX_L2P_SSTX2N	LANE 2
B2	TX2+	ML0+	ML0+	ML3+	SSTX+	4	ML2_N	A5	RX_L2N_SSTX2P	
A10	RX2-	ML1-	ML1-	ML2-	SSRX-	3	ML3_P	B3	RX_L3P_SSRX2N	LANE 3
A11	RX2+	ML1+	ML1+	ML2+	SSRX+	1	ML3_N	A3	RX_L3N_SSRX2P	

If the UFP connector in the system is DP, then all the UFP interface signals are routed to the connector, if the UFP connector is USB Type-C then only the high-speed lanes are routed connector, HPD may connect to the PD controller or remain unused. The AUX signal shall use the AC-coupling capacitors and 1M termination (Pull-up on AUX_CH_P and Pull-down on AUX_CH_N). The HPD out is a 1.8V TTL signal, it shall use 100K pull-down to GND. The KTM5030 can be powered from the connected DP or USB Type-C source or from an external power supply depending on the application.

The AUX CH supports both native AUX transaction syntax and I2C-over-AUX transaction syntax. DP source access the EDID from the downstream sink using I2C-over-AUX transactions. EDID larger than 256 bytes can be accessed using segmented addressing mechanism specified in the E-DDC standard.

The KTM5030 supports link training with AUX transactions as specified in DP1.4A. The usage of TPS4 (Training Pattern Sequence 4) is recommended to optimize both DPTX PHY drive setting of DP source and its own DPRX EQ setting. If a DP source does not support TPS4, POST_LT_ADJ_REQ procedure is recommended as defined in DP1.4A. Once the DP source has performed link training, but later stops the main link signal transmission (for example, transitioning to the power saving state with DPCD 00600h set to 02h), another full link training is required to re-establish the link. KTM5030 also supports the link training policy defined for DP alternative mode sources. In this policy, the lane count is reduced to match the number of lanes physically connected based on the DPCD clock recovery status register [LANEx-CR_DONE].

By default, the firmware keeps DP_HPD asserted unless it is in power OFF state, regardless of whether DFP HPD input is asserted or not. The DFP HPD input status is reflected on SINK_COUNT value at DPCD 00200h. The value is 1 when the DFP_HPD input is asserted, and 0 when de-asserted. Whenever KTM5030 detects DFP_HPD input status change, it generates IRQ_HPD on the UFP_HPD line.

Other signaling requirements for UFP interface such as cable sense or power sense are supported through GPIOs.

DFP Interfaces

The KTM5030 DFP interface consists of three AV ports, one USB3.2 port and a digital audio output port.

AV Interface

The three DFP interfaces can be configured as below:

DFP	Drive Architecture	AC Coupled DP++	DC Coupled HDMI	AC Coupled HDMI
TX1	VML	Y	N	Y
TX2	CML	Y	Y	Y
TX3	VML	Y	N	Y

Each interface has 4 high speed main lanes, side band channels (AUX CH or DDC CH) and HPD inputs. The max signaling rate is 8.1Gbps per lane in AC coupling mode and 6.0Gbps in DC coupling mode. TX2 transmitter has a port determination power pin TX_CM which decides the AC or DC coupled mode of operation. For AC coupled DP++ mode TX_CM pin shall connect to 1.8 V, for DC coupled HDMI mode it is left open. The high-speed main lanes shall use 0.1µF capacitor in DP++ mode or terminated to 3.3 V by the downstream sink in HDMI mode. KTM5030 autonomously controls both TMDS character clock divide by 4 and scrambling as defined by HDMI2.0b. Differential voltage swing, pre-emphasis, edge rate, and source termination can be controlled through programming..

When a Port is used in HDMI AC-Couple mode, external level translators are not required. On- board passive circuitry on High-speed and VCM Pins allow direct connection to HDMI connectors.

Each DFP AV interface has an AUX CH and DDC CH pins. In DP++ mode these signals are routed to the DP connector using an external analog switch. The switching selection is based on the CONFIG1 signal status. In HDMI mode the DDC pins are directly connected to the HDMI connector with a pull-up to VDD33.

The HPD input on each AV interface is directly connected to the HPD from the downstream sink through DP or HDMI connector. A 47K pull-down is recommended for the HPD input.

USB3.2 Interface

The DFP USB3.2 interface has a TX and a RX differential pair supporting USB 3.2 Gen1 and Gen2 bit rate streams. This is an extension of the UFP USB interface with signal integrity enhancement. KTM5030 supports BLR (Bit-Level-Retimer for the SS mode and SRIS (Separate Reference clock Independent SSC) for SSP mode. The TX and RX pair may connect to an in-system USB hub or to a downstream facing USB connector.

Audio Interface

The audio output interface in KTM5030 can be configured to transmit audio in I2S, TDM or SPDIF format exclusively. This digital audio interface comprises of 6 multi-purpose input/output pins. Functional description of these pins is covered in the connection section. KTM5030 is capable of extracting audio from the incoming AV streams and transmit on the digital audio interface for external audio CODEC. The audio stream selection and the output format selection are configurable through firmware. In SPDIF configuration, there are 4 audio pins, each can be configured to drive 2-Channel PCM or compressed audio data from a single stream source. Maximum toggle rate in this format is limited to 50MHz. In I2S configuration 6 audio pins (4 data, bit clock, word clock) are used to drive 8-Channel audio data. In TDM format 3 audio pins (1 data, bit clock, word clock) are used to driver 8-Channel audio in time division multiplexing. The security policy engine in KTM5030 prevents transmission of protected audio through digital audio interface port.

SPI Interface

KTM5030 uses an external SPI flash memory to store the firmware. This is a standard SPI interface comprises of following signals: SPI_CSN, SPI_WPN, SPI_HOLD, SPI_DO, SPI_DI, SPI_CLK. KTM5030 supports single, dual, quad and QPI read mode operation. SPI clock speed is programmable, and the maximum supported clock speed is 75MHz. Commercial SPI flash of 16Mbit size, operating at 1.8V supply is recommended. Contact Kinetic for the list of qualified SPI flash devices.

I2C Interface

KTM5030 has an I2C master and a slave interface port for in-system connectivity with peripheral devices. It supports standard I2C protocol with maximum data rate up to 400Kbps. The I2C data and clock pins are 3.3V/5V tolerant and should connect to a 3.3 or 5V supply through an external 2.2K pull-up. The I2C master interface signals are multi-function pins; these pins can also function as operating mode configuration signals for external PD / TCPC controller. The I2C slave interface uses an ALERT signal to interrupt the external master.

The I2C slave, host interface, is initialized to accept I2C transactions directed to device identifier 0xE0-0xE7. Bootstrap 6 and 7 shall be used to select the I2C slave device identifier according to the table below:

Table 6. Bootstrap Selectable I2C Slave Device Identifiers

Bootstrap 7	Bootstrap 6	I2C Device Identifier
Low	Low	E0/E1
Low	High(1.8V)	E2/E3
High (1.8V)	Low	E4/E5
High(1.8V)	High(1.8V)	E6/E7

Chip Power-up Sequence and Reset

KTM5030 requires 0.95V, 1.8V - power supply for its operation. These power supply rails can be generated from external voltage regulators. Refer to the electrical specification section for the supply ratings and maximum power consumption of the device.Power Sequencing is not required by the SOC between the 1.8V & 0.95V Rails though there may be requirements based on specific usage (Type-C Interface). However care must be taken to ensure that ramp-up of Power Rails is greater than 100uS.

Power-On Reset

The Power-On Reset unit generates an internal chip reset under two conditions:

One, when the both 1.8V and 0.95V supply voltages cross the threshold level.

Two, when the RESETN signal to the chip is held low for certain duration and released.

The figure below shows internal reset signal generation in relation to the power supply threshold, ramp-up sequence and RESETN signal timing. During rail power up, the voltage (pull-up resistor to 1.8V supply) on RESETN pin is sensed by the internal Power-On Reset (POR) circuit to generate an internal reset pulse. The internal reset pulse is low until both the 1.8V and 0.95V rails are stable and continues to stay low for at least 1.5ms after the 0.95V power rail reaches 0.675Vand the 1.8V power rail reaches 1.35V (nominal threshold levels). During the device power up, the 1.8V supply should lead the 0.95V supply (VDD18 >= VDDP9 for t > 0).

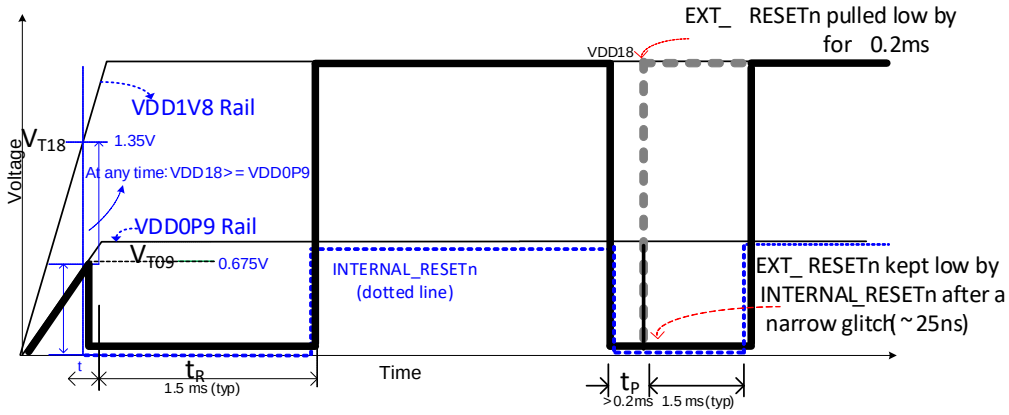


Figure 8. Power-up and Reset Timing Sequence

Any time a power supply glitch causes the power rails to fall below the nominal threshold voltage levels, the internal reset signal drops and stays low for at least 1.5ms after both power rail exceed their nominal threshold voltage levels again.

The external reset signal pin RESETN should be connected to 1.8V power supply through a 2.2K resistor. The RESETN pin may be driven by an external open-collector drive or push-button switch to assert a chip reset. A 10pF external capacitor is recommended at the RESET pin to keep the external reset signal low at least 0.2ms to generate proper chip reset.

RESETn pin is input/output open-drain analog pad, therefore it require external pull-up resistor to 1.8V/3.3V.

RESETn is an “Active-LOW” signal.

IO Pad behavior as open-drain Output pad:

- Chip can drive RESETn pin either “LOW” or “Hi-Z”
- During power ramp-up, RESETn pad is used as status pin.
- It is weakly pulled High (follows the power rail) by external resistor, once power rails reached set thresholds internal driver pulls it Low and chip enters in Reset mode.
- After ~1.5mS reset is de-asserted switching-off the internal driver and RESETn pin is pulled High by external resistor, chip comes out of reset mode and ready for normal operation.
- Leakage current when driver is off ~20nA – 100nA depending on process corner and junction temp

IO Pad behavior as Input pad:
- Internal driver is off, RESETn is High (pulled up by external resistor) and chip is in normal mode of operation
- When External Reset is required, LOW pulse should be applied to RESETn externally
- RESETn input pulse is processed through input buffer and generates a reset signal to core.
- For input buffer to detect signal as Low, voltage at RESETn pin <0.4V

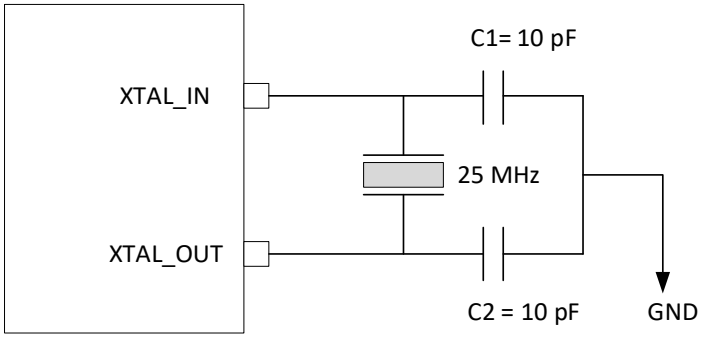
Logic delay from RESETn Low to reset signal generation is 0.2ms, therefore, external source should keep RESETn Low for at least 0.2ms

Clock Generation

KTM5030 requires an external clock signal of 25MHz for its operation. This is the reference clock for all internal clock generation. The reference clock signal can be from an external source (oscillator) to the XTAL_IN input pin or generated by the internal oscillator using a reference 25MHz crystal connected across XTAL_IN and XTAL_OUT pins. The selection between external clock input and the internal oscillator is decided through bootstrap selection pin. Refer to bootstrap configuration selection in following section. The REFCLK_OUT pin provides the internally generated reference clock signal to be used for driving 2nd KTM5030 or another device in the same system. The REFCLK_OUT is enabled or disabled through bootstrap selection pin.

Internal Oscillator Operation

A crystal resonator is connected between the XTAL_IN and XTAL_OUT pins with the appropriate capacitors (C1 and C2) to match the proper value of loading capacitance specified in crystal specification. A 25MHz crystal oscillation is necessary to meet the reference clock frequency requirement of KTM5030



Note: The value of C1 and C2 are determined based on the loading capacitance from the crystal specification and by compensating for the parasitic capacitance of the device and the printed circuit board traces. The external capacitors are terminated to GND. This connection increases the power supply rejection ratio when compared to terminating the loading capacitors to VDD.

Figure 9. Internal Oscillator with External Crystal

Crystal Specifications

While the selection of a crystal mainly depends on the specific PCB layout and the crystal manufacturer's specifications, the following are general recommendations.

Table 7. Crystal Specifications

Parameters	Specifications
Frequency	25.000MHz
Operation Mode	Fundamental
Operating Temperature	-10ºC to +70ºC
Frequency Tolerance @ 25ºC	±50ppm max
Equivalent series resistance	≤ 60Ω

Note these details of the oscillator circuit design when using a crystal resonator:

- The PCB traces should be as short as possible.
- The crystal should be a parallel resonate-cut

Functional Description

Connections

Pin List[11]

I/O Legend: I = Input; O = Output; P = Power; G = Ground; I/O = Bi-directional; AI = Analog Input

Table 8. UFP Combo Receiver/Transmitter Pins

Pin	Assignment	I/O	VDD Domain	Description
A3	RX_L3N_SSRX2P	I	0.95V	UFP combo RX/TX input. Connect to DP main lane 3 negative pin of DP connector or RX2 positive pin of USB-C connector. Use AC-coupling capacitor.
B3	RX_L3P_SSRX2N	I	0.95V	UFP combo RX/TX input. Connect to DP main lane 3 positive pin of DP connector or RX2 negative pin of USB-C connector. Use AC-coupling capacitor.
A5	RX_L2N_SSTX2P	IO	0.95V	UFP combo RX/TX input/output. Connect to DP main lane 2 negative pin of DP connector or TX2 positive pin of USB-C connector. Use AC-coupling capacitor.
B5	RX_L2P_SSTX2N	IO	0.95V	UFP combo RX/TX input/output. Connect to DP main lane 2 positive pin of DP connector or TX2 negative pin of USB-C connector. Use AC-coupling capacitor.
B10	RX_L1N_SSTX1N	IO	0.95V	UFP combo RX/TX input/output. Connect to DP main lane 1 negative pin of DP connector or TX1 negative pin of USB-C connector. Use AC-coupling capacitor.
A10	RX_L1P_SSTX1P	IO	0.95V	UFP combo RX/TX input/output. Connect to DP main lane 1 positive pin of DP connector or TX1 positive pin of USB-C connector. Use AC-coupling capacitor.
B12	RX_L0N_SSRX1N	I	0.95V	UFP combo RX/TX input. Connect to DP main lane 0 negative pin of DP connector or RX1 negative pin of USB-C connector. Use AC-coupling capacitor.
A12	RX_L0P_SSRX1P	I	0.95V	UFP combo RX/TX input. Connect to DP main lane 0 positive pin of DP connector or RX1 positive pin of USB-C connector. Use AC-coupling capacitor.
D4	RX_AUXP_SBU2	IO	1.8V	Connect to Side Band Use signal 2 pin of PD controller or connect to auxiliary channel positive pin of DP connector. Use AC-coupling capacitor.
D3	RX_AUXN_SBU1	IO	1.8V	Connect to Side Band Use signal 1 pin of PD controller or connect to auxiliary channel negative pin of DP connector. Use AC-coupling capacitor.
A1	HPD_OUT_GPIO2	O	1.8V	UFP HPD signal pin (to DP source), to be externally pulled down (100KΩ).
A7	RX_REXT	I	0.95V	Termination calibration reference resistor; 5.62KΩ 1% resistor must be connected from this pin to GND

Table 9. DFP USB Receiver/Transmitter Pins

Pin	Assignment	I/O	VDD Domain	Description
B14	TX0_SSRX_N	I	0.95V	DFP USB port pin. USB3.2 receiver negative input
A14	TX0_SSRX_P	I	0.95V	DFP USB port pin. USB3.2 receiver positive input
B16	TX0_SSTX_N	O	0.95V	DFP USB port pin. USB3.2 transmitter negative output
A16	TX0_SSTX_P	O	0.95V	DFP USB port pin. USB3.2 transmitter positive output

11. Some pins can have multiple functionalities, which are configured under register control. The alternate functionality for each pin is listed in the Description column

Table 10. DFP DP++ Transmitter Pins[12]

Pin	Assignment	I/O	VDD Domain	Description
N1	TX1_L3_HDMICLK_N	O	0.95V	DFP TX1 port pin. DP transmitter main lane 3 negative output or HDMI transmitter CLOCK negative output.
P1	TX1_L3_HDMICLK_P	O	0.95V	DFP TX1 port pin. DP transmitter main lane 3 positive output or HDMI transmitter CLOCK positive output.
R1	TX1_L2_HDMICH0_N	O	0.95V	DFP TX1 port pin. DP transmitter main lane 2 negative output or HDMI transmitter data CH0 negative output.
T1	TX1_L2_HDMICH0_P	O	0.95V	DFP TX1 port pin. DP transmitter main lane 2 positive output or HDMI transmitter data CH0 positive output.
U1	TX1_L1_HDMICH1_N	O	0.95V	DFP TX1 port pin. DP transmitter main lane 1 negative output or HDMI transmitter data CH1 negative output.
U2	TX1_L1_HDMICH1_P	O	0.95V	DFP TX1 port pin. DP transmitter main lane 1 positive output or HDMI transmitter data CH1 positive output.
U3	TX1_L0_HDMICH2_N	O	0.95V	DFP TX1 port pin. DP transmitter main lane 0 negative output or HDMI transmitter data CH2 negative output.
U4	TX1_L0_HDMICH2_P	O	0.95V	DFP TX1 port pin. DP transmitter main lane 0 positive output or HDMI transmitter data CH2 positive output.
P3	TX1_AUX_N	IO	1.8V	DFP TX1 port pin. DP transmitter Auxiliary CH negative output. Use AC-coupling capacitor.
R3	TX1_AUX_P	IO	1.8V	DFP TX1 port pin. DP transmitter Auxiliary CH positive output. Use AC-coupling capacitor.
J1	TX1_DDC_SCL	O	Open Drain, 5V TOL	HDMI TX1 DDC I2C master SCL.5V tolerant. Open drain, to be externally pulled up to DDC5V via a 1.5K ~ 2.2KΩ resistor.
H1	TX1_DDC_SDA	IO	Open Drain, 5V TOL	HDMI TX1 DDC I2C master SDA.5V tolerant. Open drain, to be externally pulled up to DDC5V via a 1.5K ~ 2.2KΩ resistor.
K1	TX1_CEC_GPIO10	IO	Open Drain, 5V TOL	HDMI TX1 CEC input.. Connect to HDMI connector CEC pin, to be externally pulled up to 3.3V via 27KΩ resistor as per HDMI1.4b specification. Use external 27KΩ pull up when CEC is not used.
K2	TX1_HPD_IN	I	Open Drain, 5V TOL	TX1 HPD input. 5V tolerant. Connect to HDMI connector HPD pin. To be externally pulled down via 47KΩ resistor. Can be used as Interrupt (Alert) input when the TX1 port is configured USB Type-C Altmode.
D16	TX1_CONFIG1_GPIO11	I	Open Drain, 5V TOL	TX1 Config1 input. Programmable Slew Rate and Drive Strength when this is being used as a GPIO.
T6	TX2_L3_HDMICLK_N	O	0.95V	DFP TX2 port pin. DP transmitter main lane 3 negative output or HDMI transmitter CLOCK negative output.
U6	TX2_L3_HDMICLK_P	O	0.95V	DFP TX2 port pin. DP transmitter main lane 3 positive output or HDMI transmitter CLOCK positive output.
U7	TX2_L2_HDMICH0_N	O	0.95V	DFP TX2 port pin. DP transmitter main lane 2 negative output or HDMI transmitter data CH0 negative output.
U8	TX2_L2_HDMICH0_P	O	0.95V	DFP TX2 port pin. DP transmitter main lane 2 positive output or HDMI transmitter data CH0 positive output.
U9	TX2_L1_HDMICH1_N	O	0.95V	DFP TX2 port pin. DP transmitter main lane 1 negative output or HDMI transmitter data CH1 negative output.
U10	TX2_L1_HDMICH1_P	O	0.95V	DFP TX2 port pin. DP transmitter main lane 1 positive output or HDMI transmitter data CH1 positive output.
U11	TX2_L0_HDMICH2_N	O	0.95V	DFP TX2 port pin. DP transmitter main lane 0 negative output or HDMI transmitter data CH2 negative output.
T11	TX2_L0_HDMICH2_P	O	0.95V	DFP TX2 port pin. DP transmitter main lane 0 positive output or HDMI transmitter data CH2 positive output.
M3	TX2_AUX_N	I/O	1.8V	DFP TX2 port pin. DP transmitter Auxiliary CH negative output. Use AC-coupling capacitor.

12. The HDMI TX output is terminated at the receiver through a 50Ω resistor

Pin	Assignment	I/O	VDD Domain	Description
N3	TX2_AUX_P	I/O	1.8V	DFP TX2 port pin. DP transmitter Auxiliary CH positive output. Use AC-coupling capacitor.
G1	TX2_DDC_SCL	O	Open Drain, 5V TOL	HDMI TX2 DDC I2C master SCL. 5V tolerant. Open drain, to be externally pulled up to DDC5V via a 1.5K ~ 2.2KΩ resistor.
H2	TX2_DDC_SDA	IO	Open Drain, 5V TOL	HDMI TX2 DDC I2C master SDA 5V tolerant. Open drain, to be externally pulled up to DDC5V via a 1.5K ~ 2.2KΩ resistor.
L2	TX2_CEC_GPIO37	IO	Open Drain, 5V TOL	HDMI TX2 CEC input. Connect to HDMI connector CEC pin, to be externally pulled up to 3.3V via 27KΩ resistor as per HDMI1.4b specification. Use external 27KΩ pull up when CEC is not used.
J2	TX2_HPD_IN	I	Open Drain, 5V TOL	TX2 HPD input., 5V tolerant. Connect to HDMI connector HPD pin. To be externally pulled down via 47KΩ resistor. Can be used as Interrupt (Alert) input when the TX2 port is configured USB Type-C Altmode.
H17	TX2_CONFIG1_GPIO12	I	1.8V	TX2 Config1 input.. Programmable Slew Rate and Drive Strength when this is being used as a GPIO.
U13	TX3_L3_HDMICLK_N	O	0.95V	DFP TX3 port pin. DP transmitter main lane 3 negative output or HDMI transmitter CLOCK negative output.
U14	TX3_L3_HDMICLK_P	O	0.95V	DFP TX3 port pin. DP transmitter main lane 3 positive output or HDMI transmitter CLOCK positive output.
U15	TX3_L2_HDMICH0_N	O	0.95V	DFP TX3 port pin. DP transmitter main lane 2 negative output or HDMI transmitter data CH0 negative output.
U16	TX3_L2_HDMICH0_P	O	0.95V	DFP TX3 port pin. DP transmitter main lane 2 positive output or HDMI transmitter data CH0 positive output.
U17	TX3_L1_HDMICH1_N	O	0.95V	DFP TX3 port pin. DP transmitter main lane 1 negative output or HDMI transmitter data CH1 negative output.
T17	TX3_L1_HDMICH1_P	O	0.95V	DFP TX3 port pin. DP transmitter main lane 1 positive output or HDMI transmitter data CH1 positive output.
R17	TX3_L0_HDMICH2_N	O	0.95V	DFP TX3 port pin. DP transmitter main lane 0 negative output or HDMI transmitter data CH2 negative output.
P17	TX3_L0_HDMICH2_P	O	0.95V	DFP TX3 port pin. DP transmitter main lane 0 positive output or HDMI transmitter data CH2 positive output.
P15	TX3_AUX_N	IO	1.8V	DFP TX3 port pin. DP transmitter Auxiliary CH negative output. Use AC-coupling capacitor.
R15	TX3_AUX_P	IO	1.8V	DFP TX3 port pin. DP transmitter Auxiliary CH positive output. Use AC-coupling capacitor.
E1	TX3_DDC_SCL	O	3.3V, 5V TOL	HDMI TX3 DDC I2C master SCL. 3.3V logic level, 5V tolerant. Open drain, to be externally pulled up to DDC5V via a 1.5K ~ 2.2KΩ resistor.
G2	TX3_DDC_SDA	IO	3.3V, 5V TOL	HDMI TX3 DDC I2C master SDA. 3.3V logic level, 5V tolerant. Open drain, to be externally pulled up to DDC5V via a 1.5K ~ 2.2KΩ resistor.
L1	TX3_CEC_GPIO36	IO	3.3V, 5V TOL	HDMI TX3 CEC input. 3.3V open drain IO. Connect to HDMI connector CEC pin, to be externally pulled up to 3.3V via 27KΩ resistor as per HDMI1.4b specification. Use external 27KΩ pull up when CEC is not used.
F1	TX3_HPD_IN	I	3.3V, 5V TOL	TX3 HPD input. 3.3V logic level, 5V tolerant. Connect to HDMI connector HPD pin. To be externally pulled down via 47KΩ resistor. Can be used as Interrupt (Alert) input when the TX3 port is configured USB Type-C Altmode.
J17	TX3_CONFIG1_GPIO13	I	1.8V	TX3 Config1 input. 1.8V logic. Programmable Slew Rate and Drive Strength when this is being used as a GPIO.

Table 11. System Interface Pins

Pin	Assignment	I/O	VDD Domain	Reset State	Description
B7	RESETN	IO	1.8V	Input	Power-ON chip reset (active low) input signal. Can be driven low by an external reset signal. Use external pull up to 1.8V power rail via 2.2KΩ +/-10% resistor.
A8	REFCLK_OUT	O	1.8V	Output	Reference clock output (25MHz). Can be used as clock source for external devices on the system.
C7	XTAL_IN	IO	1.8V	Input/ Output	Crystal node. Connect to 25MHz crystal with 10pF to GND. When the oscillator clock is used as reference, connect to the clock.
C8	XTAL_OUT	IO	1.8V	Input/ Output	Crystal node. Connect to 25MHz crystal with 10pF to GND. When the oscillator clock is used as reference, this pin is NC.
R5	TX1_CM	IO	1.8V	Input/ Output	TX1 VML port determination/power pin: AC-coupled mode only (DP, DP++, HDMI); capacitor filtering to GND needed.
R8	TX2_CM	IO	1.8V	Input/ Output	TX2 CML port determination/power pin: For AC-coupled mode (DP, DP++ HDMI) this pin must be connected to 1.8 V with proper capacitor filtering to GND. For DC-coupled more (HDMI only), only capacitor filtering to GND needed.
R12	TX3_CM	IO	1.8V	Input/ Output	TX3 VML port determination/power pin: AC-coupled mode only (DP, DP++, HDMI); capacitor filtering to GND needed.
E2	I2C_SDA_GPIO0	IO	Open Drain, 5V TOL	Input, Internal PU	Configurable Slave or Master I2C interface data line up to 400kbps. Programmable Slew Rate and Drive Strength when this is being used as GPIO.
F2	I2C_SCL_GPIO1	IO	Open Drain, 5V TOL	Input, internal PU	Configurable Slave or Master I2C interface data line up to 400kbps. Programmable Slew Rate and Drive Strength when this is being used as GPIO.
F16	SPI_CSN	O	1.8V	output, Internal PU	Serial peripheral interface chip select. Programmable Slew Rate and Drive Strength.
F17	SPI_DI	IO	1.8V	Input, Internal PD	Serial peripheral interface data input. Use as DQ1 input/output during quad mode operation.
D17	SPI_DO	IO	1.8V	Output, Internal PU	Serial peripheral interface data output. Use as DQ0 input/output during quad mode operation.
E16	SPI_CLK	IO	1.8V	Output, Internal PD	Serial peripheral interface clock.
G16	SPI_WPN	IO	1.8V	Input, Internal PD	Serial peripheral interface write protect. Use as DQ2 input/output during quad mode operation.
E17	SPI_HOLD	IO	1.8V	Input, Internal PU	Serial peripheral interface hold signal. Use as DQ3 input/output during quad mode operation.
G17	URX_GPIO8	I	1.8V	Input, Internal PU	Universal asynchronous serial RX input. Internal PU. Can be used as GPIO. Programmable Slew Rate and Drive Strength.
H16	UTX_GPIO9	O	1.8V	Input, Internal PD	Universal asynchronous serial TX output. Can be used as GPIO. Programmable Slew Rate and Drive Strength
D1	I2CM_SDA_PCONF0	IO	Open Drain, 5V TOL	Input Internal PD	I2C Master interface data line up to 400kbps or Bit 0 of operating mode configuration pin. Can be used as GPIO. Programmable Slew Rate and Drive Strength.

Pin	Assignment	I/O	VDD Domain	Reset State	Description
B1	I2CM_SCL_PCONF1	IO	Open Drain, 5V TOL	Input Internal PD	I2C Master interface clock line up to 400kbps or Bit 1 of operating mode configuration pin. Can be used as GPIO. Programmable Slew Rate and Drive Strength.
C1	ALERTN_PPOL	IO	Open Drain, 5V TOL	Input Internal PD	Interrupt (Alert) input or USB Type-C plug orientation configuration pin Low: normal operation, High: flipped operation
J16	GPIO6	IO	1.8V	Input Internal PD	General Purpose IO. Programmable Slew Rate and Drive Strength.
K17	GPIO7	IO	1.8V	Input Internal PU	General Purpose IO. Programmable Slew Rate and Drive Strength.
K16	I2S_WCK_GPIO14	IO	1.8V	Input Internal PU	I2S Audio word clock. Can be used as GPIO. Programmable Slew Rate and Drive Strength.
L17	I2S_FCK_GPIO15	IO	1.8V	Input Internal PD	I2S Audio bit clock. Can be used as GPIO. Programmable Slew Rate and Drive Strength.
L16	I2S_D0_GPIO16	IO	1.8V	Input Internal PU	I2S Audio data bit 0 OR SPDIF audio output 0. Can be used as GPIO. Programmable Slew Rate and Drive Strength.
M17	I2S_D1_GPIO17	IO	1.8V	Input Internal PU	I2S Audio data bit 1 OR SPDIF audio output 1. Can be used as GPIO. Programmable Slew Rate and Drive Strength.
M15	I2S_D2_GPIO18	IO	1.8V	Input Internal PU	I2S Audio data bit 2 OR SPDIF audio output 2. Can be used as GPIO. Programmable Slew Rate and Drive Strength.
M16	I2S_D3_GPIO19	IO	1.8V	Input Internal PU	I2S Audio data bit 3 OR SPDIF audio output 3. Can be used as GPIO. Programmable Slew Rate and Drive Strength.
D15	NC	IO	-	NA	Leave as NC
G15	TEST	IO	-	NA	Test purpose. Connect to GND

Table 12. Power and Ground Pins

Pin	Assignment	Voltage Level	Description
D5, D6, D7, D8, D9, D10, D11, D12, D13	AVDDP9_UFP	0.95V	Combo RX analog power
P4, P5, P6, P7, P8, P9, P10, P11, P12, P13	AVDDP9_TX	0.95V	DisplayPort TX analog power
E4, E14, F4, F14, G4, G14, H4, H14, J4, J14, K4, K14, L4, L14, M4, M14	DVDDP9	0.95V	Core 0.95V power
C10, C11, C12, C13	AVDD18_UFP	1.8V	Combo RX analog power
R4, R6, R7, R9, R10, R11, R13	AVDD18_TX	1.8V	DisplayPort TX analog power
E15, F15, G3, H3, H15, J15, K15, L15	DVDD18	1.8V	1.8V IO power
A2, A4, A6, A9, A11, A13, A15, A17, B2, B4, B6, B8, B9, B11, B13, B15, B17, C[2:6], C9,17 C16,C17, D2, D14, E3, E[5:13], F3, F[5:13], G[5:13],H[5:13],J3, J[5:13], K3,K[5:13], L3, L[5:13],M1,M2, M[5:13], N2, N[4:13], N[15:17], P2, P16, R2, R14, R16, T[2:5], T[7:10], T[12:16], U5, U12	GND	GND	Power return for all supplies

Bootstrap Configuration

DC levels on the bootstrap pins shown below are latched during the de-asserting edge of power-on reset (RESETN goes HIGH).

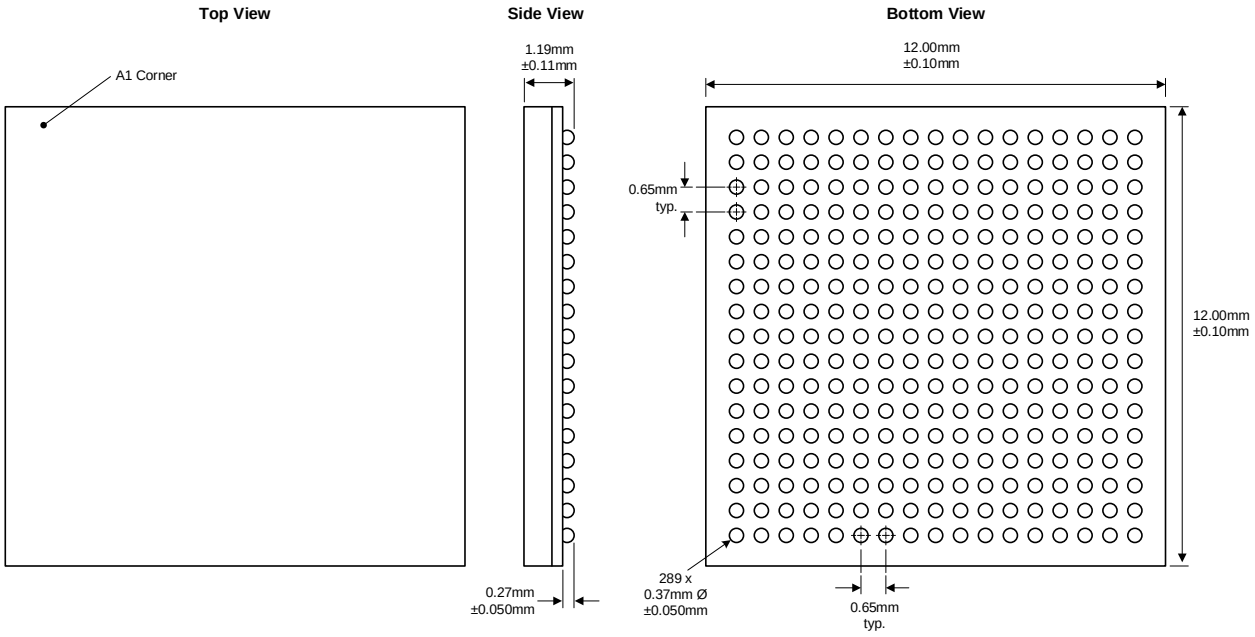
Table 13. Bootstrap Configuration[13]

Bootstrap Signal Name	Assignment	VDD Domain	Internal PU/PD	Function
Bootstrap ‘0’	I2S_FCK_GPIO15 (L17)	1.8V	PULL DOWN	Internal. Leave as NC for normal operation.
Bootstrap ‘1’	I2S_D3_GPIO19 (M16)	1.8V	PULL DOWN	Ref clock out select. 0 – Enable (Default) 1 – Disable
Bootstrap ‘2’	SPI_CLK (E16)	1.8V	PULL DOWN	Internal. Leave as NC for normal operation.
Bootstrap ‘3’	I2S_WCK_GPIO14 (K16)	1.8V	PULL DOWN	Internal. Leave as NC for normal operation.
Bootstrap ‘4’	SPI_DO (D17)	1.8V	PULL UP	Reference clock select 1 – Crystal Oscillator 0 – External TCLK
Bootstrap ‘5’	UTX_GPIO9 (H16)	1.8V	PULL UP	Internal. Leave as NC for normal operation.
Bootstrap ‘6’	I2S_D0_GPIO16 (L16)	1.8V	PULL UP	Can be used for customized application configuration.
Bootstrap ‘7’	I2S_D1_GPIO17 (M17)	1.8V	PULL UP	Can be used for customized application configuration.
Bootstrap ‘8’	I2S_D2_GPIO18 (M15)	1.8V	PULL UP	Internal. Leave as NC for normal operation.

13. When the pin corresponding to a specific bootstrap is left NC, the pin takes the value of the assigned by the internal PULL UP (Level 1) or PULL DOWN (Level 0). The internal resistor used for 1.8V IO is around 80-95KΩ. To select a non-default value on a bootstrap, use an external PULL UP or PULL DOWN resistor tied to the opposite direction that overcomes the internal PULL UP or PULL DOWN. Recommended external PULL UP resistor (14 -16KΩ), PULL DOWN resistor 2.2KΩ.

Packaging Information

LFBGA1212-289 (12.00mm x 12.00mm x 1.30mm)



Recommended Footprint