Application Note AN004

Design Guide for the AS1113 PoE Powered Device

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INTRODUCTION

ABOUT THIS DESIGN GUIDE

This design guide provides some general guidelines to be used when you are designing with the AS1113 Powered Device (PD) Controller. It is to be used in conjunction with the datasheet and reference design. The design guide provides guidelines for adapting the reference design to a customer's system. If there are any questions of concerns please contact the Kinetic applications team through your sales contact or info@kinet-ic.com.

SCHEMATIC CONSIDERATIONS

ETHERNET LINE SIDE

The Center Tap (CT1, CT2) and Signal Path (SP1, SP2) signals should be directly connected to the center taps on the RJ45 side of the Ethernet line transformer. IEEE 802.3af-compliant system will use either Alternative A or Alternative B power connectivity, with power supplied on CT1 & CT2, or SP1 & SP2 respectively. Although the AS1113 doen't differentiate between the pairs, for design flexibility, we recommend that the designer use the IEEE connectivity.

Since the center-tap transformer connections do not carry data traffic, these traces can be wider on the board and increased width is recommended to carry the relatively large current (up to 1A).

DC-DC CONVERTER

A π filter should be employed on the VDD48O pin to reduce the amount of noise on the line. The following filter is recommended between the PD VDD48O pin and transformer primary winding node.

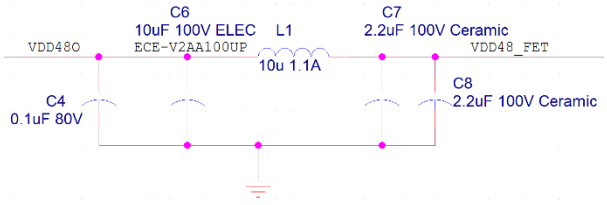


Figure 1: π Filter

Also any device connected to VDD48O should be rated to handle 80V and at least 2A.

The AS1113 support isolated forward, flyback and non-isolated buck DC-DC topologies. Information on the different topologies can be found in the corresponding datasheets.

The designer should also decide whether the system needs power isolation. If the system is non-isolated, the high voltage and low voltage grounds should be shorted together.

If the system is isolated, an opto-coupler is needed on the feedback line. This ensures that no DC path connects the two sides of the board. To reduce common-mode noise on the Ethernet lines, a 4700pF, 2KV cap is recommended between the PoE ground and board ground.

802.3af/at COMPLIANCE

Two pins, RCURR and RCLASS are used for programming the PD compliance levels in the AS1113.

The RCURR pin should be shorted to ground, resulting in anominal current limit of 400mA.

User-programmable classification current levels are set by RCLASS pin. Each class represents a power allocation level for a PD, so that PSE can manage power between multiple PDs. The recommended resistance values for the RCLASS pins can be found in Table 1. More information on their use can be found in the datasheet.

Table 1. Classification Resistors

Class	Power (Watts)	I_{Class}	R_{class}
0	0.44-12.95	0-4 mA	Pull-up
1	0.44-3.84	9-12 mA	280k Ω
2	3.84-6.49	17-20 mA	143k Ω
3	6.49-12.95	26-30 mA	90.9k Ω
4	Reserved	36-44 mA	63.4k Ω

COMPONENT PLACEMENT CONSIDERATIONS

Appendix A shows example evaluation board schematics for a Power Splitter design with Isolated Forward DC-DC Converter. Example layouts from this board are used to illustrate desirable design and layout practices through rest of this document.

ETHERNET SIGNALS

No special placement consideration is required for the Ethernet line components using the AS1113. In general the PD device should be placed as close to the center tap of the transformer as possible to limit IR drop.

DC-DC CONVERTER

If using a Forward or Flyback Topology, the NDRV, PDRV FETs, and their associated protection diodes should be placed as close to the PD Controller as possible. If possible, place them on the reverse side of the board. The DC-DC transformer should be placed on the top of the board to limit the distance between the switching FETs and the transformer.

When using in a buck topology, the FET and the inductor should be placed as close to the PD Controller as possible.

Figures 2 and 3 shows an example component placement of the top and bottom of a board.

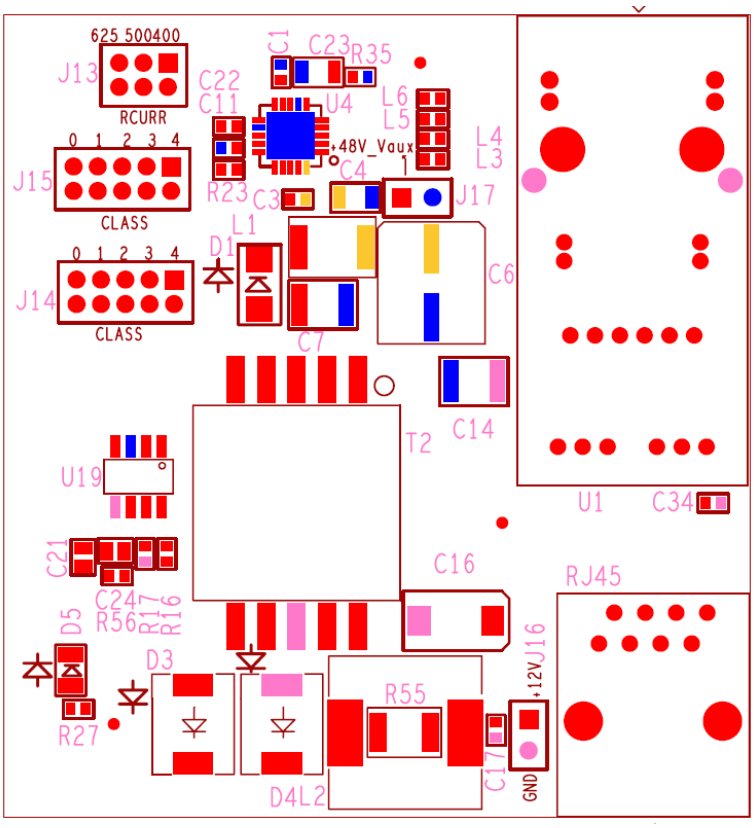


Figure 2: Top Side Component Placement

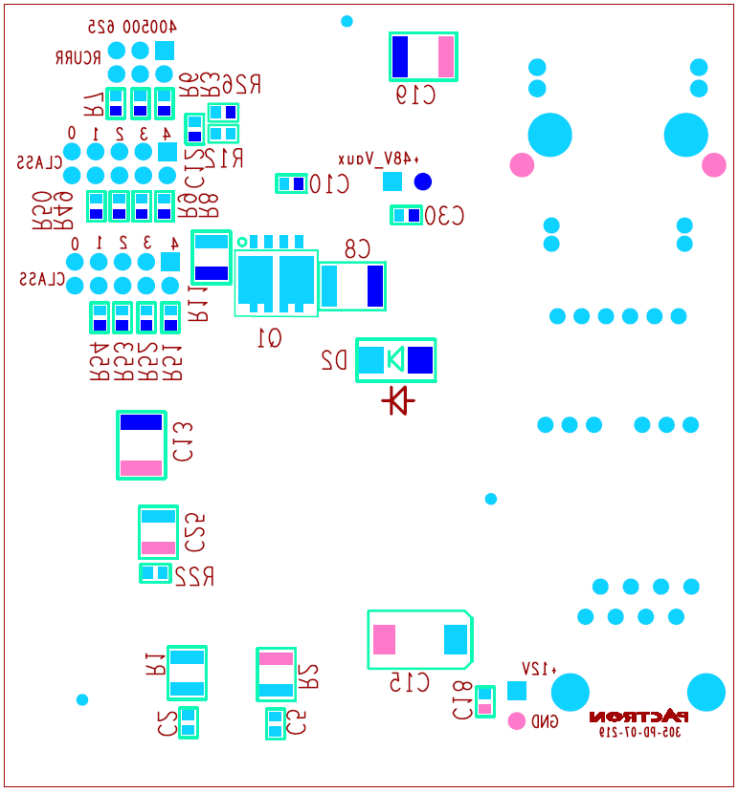


Figure 3: Bottom Side Component Placement

LAYOUT CONSIDERATIONS

ETHERNET SIGNALS

Ethernet signal layout on the secondary side of the input transformer should follow recommendation from the PHY supplier. The AS1113 does not require additional considerations.

In general, Ethernet data signals are high frequency differential signaling channels. Their routing should reflect 100Ω differential impedance on both sides of the input transformer. They should avoid sharp bends and sudden width changes as this affects the impedance and current carrying capacity of the lines. They should have appropriate ground planes underneath them for both common-mode signal return and to shield against coupled noise from the DCDC converter.

The grounds should be solid without islands or choke points to ensure low impedance return path.

High speed signals should be routed away from the DC-DC converter to avoid the converter switching noise appearing on the data lines.

In general the center tap and transformer input signals (CT1, CT2, SP1 and SP2) should be 50mils wide to minimize the IR drop for the relatively large current to & from the line.

DC-DC CONVERTER

VDD48O signal routing should be at least 200 mils wide and all components directly connected to it should also be 200 mils wide including routing to the drain and gates of the FETs between NDRV, PDRV and the primary side of the transformer.

Traces attached to the secondary side of the converter should be appropriate for the output current of the DCDC converter. For max power delivery, it is recommended that a line-width of >200mils be used. Any layer transitions for these high-power signals require multiple vias to ensure low inductance and resistance.

The length of all high impedance small signal traces should be kept to a minimum and shielded from any switching power traces.

Ceramic by pass capacitors C3 and C10 should be places as close as possible to the PD Controller for optimum sourcing of the switching current associated with the gate drive of the high side

and low side power MOSFETs. This will assist in minimizing the high frequency ringing and ripple at VBP and VBN of the AS1113.

The AS1113 paddle should tie directly to the return of C7 and C8 in a path that does not share the high power current associated with the DC-DC converter.

Minimizing the loop area for all high frequency switching currents helps to reduce radiated EMI. Ceramic capacitors C7 and C8 supply the high frequency switching current for the primary side of the integrated converter block in the PD Controller. The loop of C7 and C8 connects to Q1-S_P and the cathode of D1 with the return path tying to the current sense resistor R11. This loop area should be minimized.

THERMAL PAD

The Kinetic-recommended 5x5mm 20-LD QFN footprint for the AS1113 package should be followed. It is essential that the bottom-side pad be used for both thermal and electrical contact. A good solder connection to it is essential.

This pad should be filled with as many vias as practical to ensure good thermal conductivity to the board ground plane. It is also recommended that a metal pad is created on the bottom-side of the board, and it is not recommended that signals be routed underneath the part. Stack-up and General layout guidelines

For a multilayer board, ground and signal layers should be internal to the board and should separate active signals to ensure good capacitance between layers and ensure there is a good reference or return for the active signals.

GROUND LAYERS

The DC-DC converter creates isolated voltages from the high voltage signals coming from the Ethernet line. Because of this there are two grounds in the system: a high voltage and a low voltage ground. The grounds should be separated by a gap on all power and ground planes to reduce DC-DC noise coupling to the Ethernet signals. Kinetic recommends a minimum gap of 0.050”. Ground planes should use 1oz copper and should be as continuous as possible with no isolated islands and no narrow choke points.

To maintain ground separation, secondary-side components and routing should be placed over the low-voltage ground and primary-side components and routing should be placed over the high-voltage ground.

LAYOUT EXAMPLE

Figure 4 is an example layout that applies to both the AS1113.

Appendix A has the corresponding schematics the implementation of a forward isolated converter.

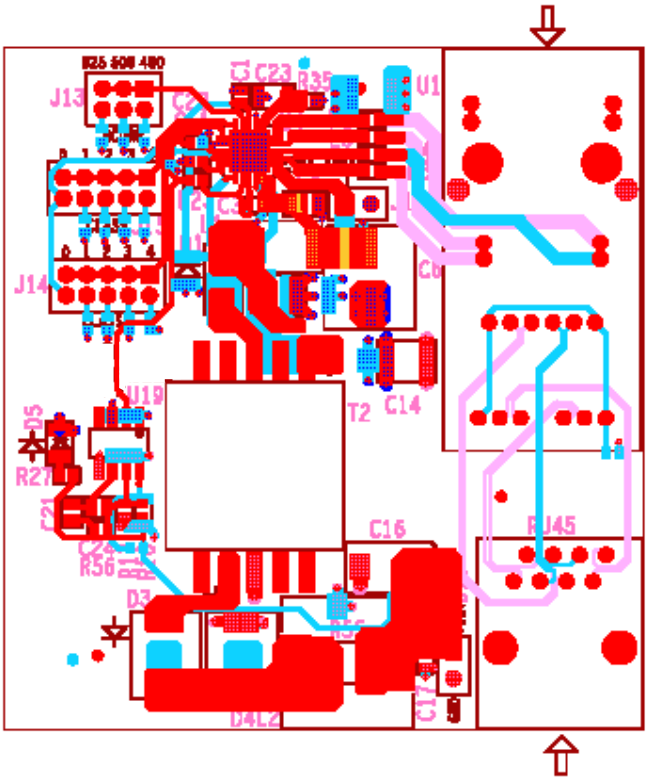


Figure 4: Layout Example

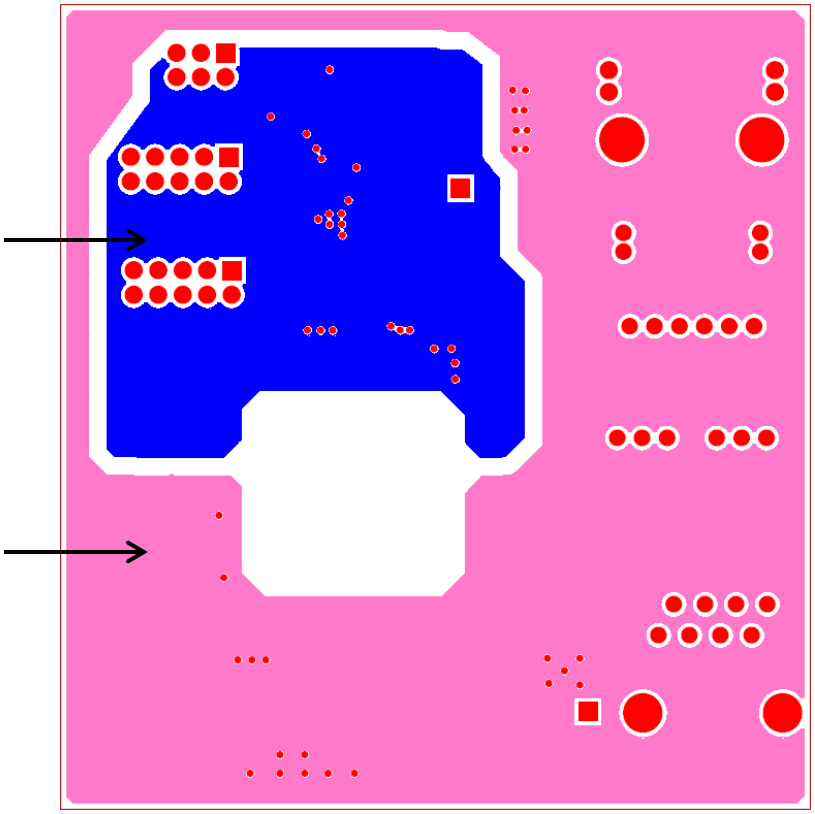
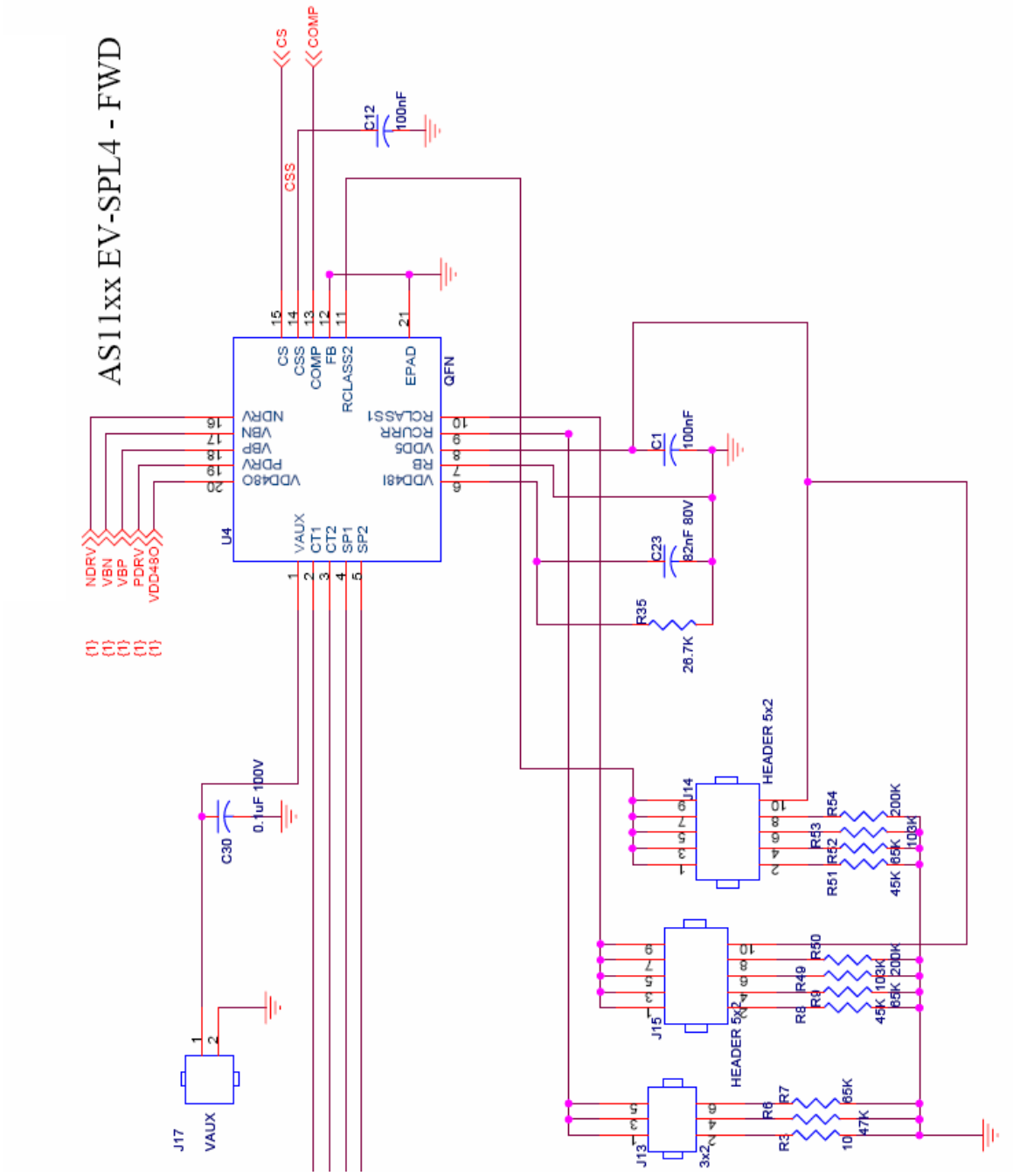
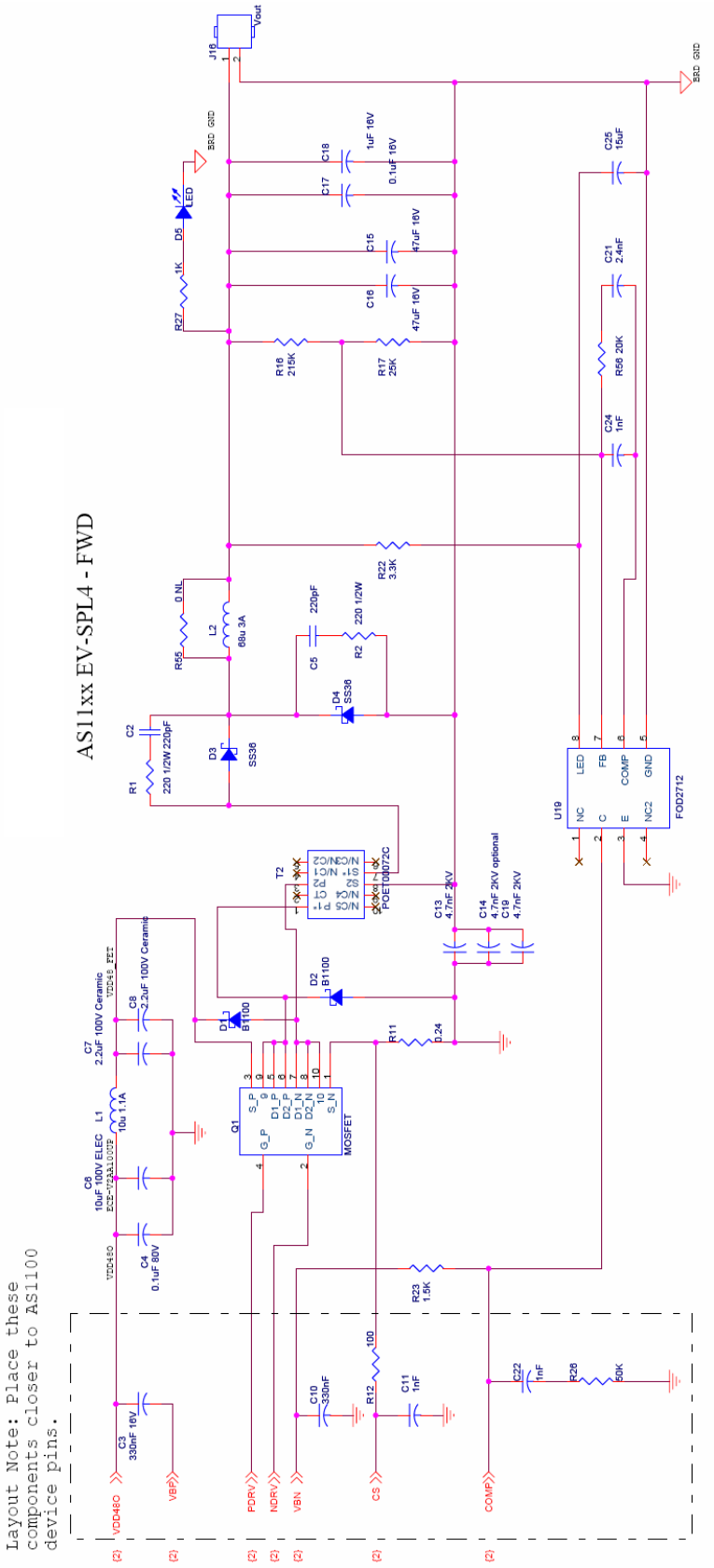


Figure 5: Recommended Ground Plane Split on the board using Mag-jack for POE port

APPENDIX A: EXAMPLE SCHEMATIC




AS11xx EV-SPL4 - FWD
Layout Note: Place these components closer to AS1100 device pins.
Vout
SEC GND
PRI GND
LED
D5
R27 1K
C18 1uF 16V
C17 0.1uF 16V
C15 47uF 16V
C16 47uF 16V
R16 215K
R17 25K
C25 15uF
C21 2.4nF
R56 20K
C24 1nF
R22 3.3K
R55 0 NL
L2 68u 3A
C5 220pF
R2 220 1/2W
D4 SS36
D3 SS36
C2 220 1/2W 220pF
R1
T2 POET0072C
U19 FOD2712
LED FB COMP GND NC NC2 C E
C13 4.7nF 2KV
C14 4.7nF 2KV optional
C19 4.7nF 2KV
D2 B1100
D1 B1100
C8 2.2uF 100V Ceramic
C7 2.2uF 100V Ceramic
R11 0.24
Q1 MOSFET
L1 10u 1.1A
C6 10uF 100V ELEC
C4 0.1uF 50V
R23 1.5K
C3 330nF 16V
C10 330nF
R12 100
C11 1nF
C22 1nF
R26 50K
VDD480
VBP
PDRV
NDRV
VBN
CS
COMP

CONTACT INFORMATION

Kinetic Technologies

6399 San Ignacio Ave, Suite 250
San Jose, CA 95119
USA

Tel: 1 (408) 746-9000

Fax: +1 (408) 351-0338

Email inquiries: info@kinet-ic.com

Website: www.kinet-ic.com

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