# IEEE 802.3bt-Compliant, Powered Device Interface Controller

## Features

- Fully supports IEEE® Std. 802.3bt
- Supports Input Power Levels Up to 90W
- Compatible with both IEEE® Std. 802.3af/at
- Support Class 0-8 for PD
- Robust Type 1, 2, 3 and 4 PSE detector with proprietary digital filtering line noise
- Auto-adjust Maintain Power Signature (MPS) for type 1-4 PSE
- Supports up to 5 Event Classification
- Programmable DC current limit up to 2.3A for 90W applications
- IEC 61000-4-2/3/4/5/6 requirements for EMC Compliance
- Exceptional EMI performance
- Low Rds-on 100 V Hot-Swap FET (typical 0.1Ω)
- Integrated Short-Circuit Protection
- Over temperature protection
- Seamless support for local power down to 9.5V
- Supports Low Power Standby Modes
- 5x5 mm, 20 lead WQFN Package
- -40°C to +125°C Junction Temperature Range

## Applications

- Pan, tilt and zoom (PTZ), security and web cameras
- Voice over IP (VoIP) phones
- Lighting and High Power Wireless Data Systems
- Wireless LAN access points, WiMAX terminals
- Point-of-sale (PoS) terminals, RFID terminals
- Thin clients and notebook computers
- Fiber-to-the-home (FTTH) terminals

## Brief Description

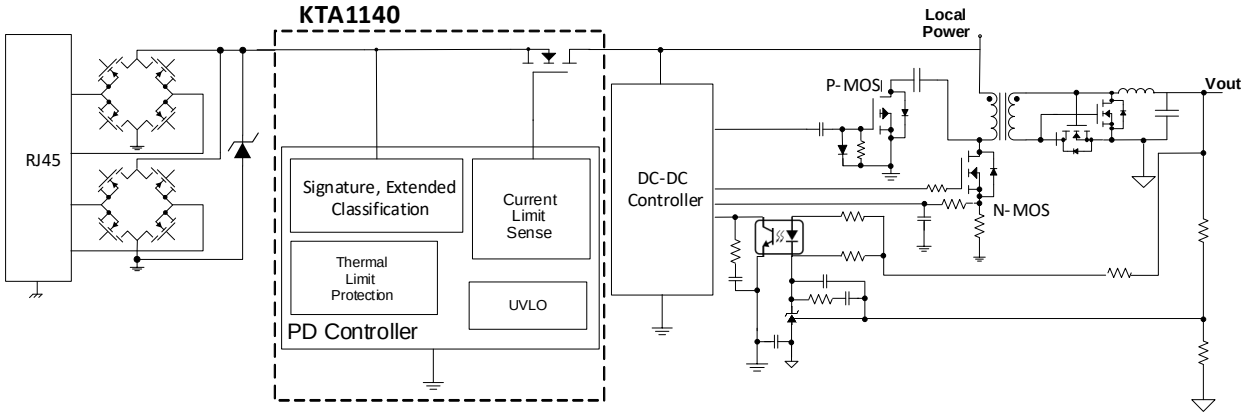
The KTA1140 is a single-chip, highly integrated CMOS solution for Power over Ethernet (PoE) Powered Devices requiring input power of up to class 8 and 90Watts. Applications include Voice over IP (VoIP) Phones, Wireless LAN Access Point, Security Cameras, WiMAX Terminals, Point-of-Sales Terminals, RFID Readers, Thin Clients and Notebook computers.

The KTA1140 implements all of the physical layer Powered Device (PD) functionality, as required by IEEE® 802.3af-2003, IEEE® 802.3at-2009 and IEEE® 802.3bt-2018 standards. This includes 5-event classification, Type 1-2 or 3-4 PSE detection indicators (PST1/2 and PSDBT), PD detection, under-voltage lockout (UVLO), and Hot-Swap FET integration.

The KTA1140 has been architected to address EM emission concerns in PoE applications. The chip implements many design features that minimize transmission of system common-mode noise onto the Unshielded Twisted Pair (UTP).

The device is designed to provide safe, low-impedance discharge paths directly to the earth ground, resulting in superior reliability and circuit protection.

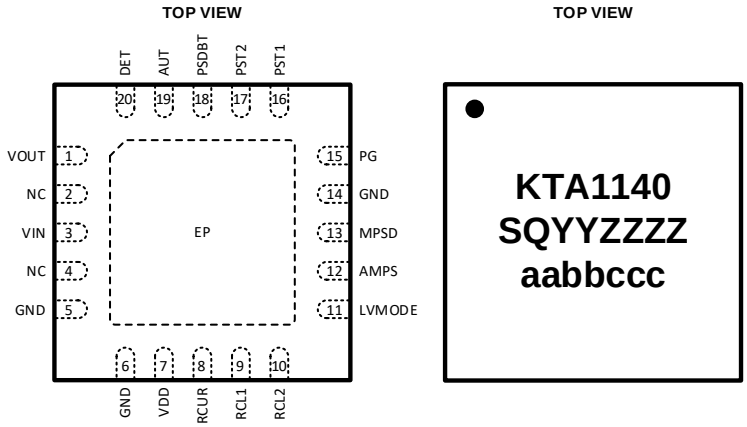
## Typical Application



## Ordering Information

| Part Number | Marking[1] | Operating Temperature | Package |
|---|---|---|---|
| KTA1140EUAQ-TB | SQYYZZZZ | -40°C to +125°C Junction Temperature | WQFN55-20 |

## Pinout Diagram




**Top Mark**
**WQFN-55-20 Package**
**(5.00mm x 5.00mm x 0.75mm)**
**SQ= Device Code, YY= Date Code, ZZZZ= Serial Number**
**aabbccc = Serial Number of Assembly Lot**

1. SQ = Device Code, YY - Date Code, ZZZZ - Serial Number.

## Pin Descriptions

| Pin # | I/O | Name | Function |
|---|---|---|---|
| 1 | P | VOUT | Switched supply output |
| 2 | - | NC | Not Connected |
| 3 | P | VIN | Positive bus pin fed by the output of the external rectification bridge. This bus requires the connection of a detection signature capacitor and resistor. Refer to Detection Mode section. |
| 4 | - | NC | Not Connected |
| 5, 6 | A | GND | Must be connected to paddle ground (GND) |
| 7 | O | VDD | Internal Voltage 5V supply output decoupling point |
| 8 | A | RCURR | Current limit pin.<br>RCURR = GND for AF, RCURR = 5kΩ for AT, RCURR = 10kΩ for BT1, RCURR = Open for BT2 |
| 9 | I | RCL1 | Connect a resistor from RCL1 to GND to program the first classification current. |
| 10 | I | RCL2 | Connect a resistor from RCL2 to GND to program the second classification current. |
| 11 | A/I | LVMODE | Local Voltage Mode. When pulled high, LVMODE opens the internal FET switch and keeps the DC-DC controller active. It should be pulled to GND when not in use. |
| 12 | I | AMPS | Automatic Maintain Power Signature (MPS) control. Connect a resistor with appropriate power rating (to support the MPS current) from AMPS to GND to program the MPS current amplitude. Leave AMPS open to disable the automatic MPS function. |
| 13 | A/I | MPSD | Maintain Power Signature (MPS) duty cycle select input, referenced to GND, internally driven by a precision current source with voltage limited to less than ~5.5V. For PSE type 3 and 4 with long class event, A resistor connected to GND determines if the MPS duty cycle selected is either 5.4% (open), 8.1% (~60.4 kΩ) or 12.5% (short). Note: For PSE type 1 and 2 with short class event, the MPSD resistor is not important. |
| 14 | O | GND | Ground; Connect it to the DC-DC controller ground. |
| 15 | O | PG | Power Good Indicator, Output, Open Drain active-low |
| 16 | O | PST1 | PSE Type Indicator. Output, Open Drain active-low, Class result LSB output. This pin is referenced to GND |
| 17 | O | PST2 | PSE Type Indicator2. Output, Open Drain active-low Class result MSB output. This pin is referenced to GND. |
| 18 | O | PSDBT | POE PSE TYPE/Power BT detects. This pin is also referenced to GND. Output, Open Drain active-low. Low level output indicates availability of PoE.BT higher system power level in Type 3 or 4. |
| 19 | A | AUT | Auto-class enable input. Internally pulled-up to internal VDD rail during classification only, pulled down in other circumstances to minimize consumption. Pull low (to GND) to enable the Auto class function during classification. Leave open otherwise. |
| 20 | A | DET | Connect a 25.5kΩ resistor from DET to VIN to provide the PoE detection signature. Pull DET to GND to disable the pass MOSFET during powered operation. |
| EP | Exposed Pad | GND | Local analog ground. This is the negative output from the external rectification bridge and is not isolated from the line input. |

Key: I = Input, O = Output, A = Analog Signal, P = Power

## Absolute Maximum Ratings[2]

(TA = 25C unless otherwise noted)

| Symbol | Description | Value | Units |
|---|---|---|---|
| VIN, VOUT, DET | High Voltage Pins[3] | 100 | V |
| VDD, , RCL1,2, LVM, RCUR, AUT, AMPS, MPSD, PG, PST1/2, PSDBT | Low Voltage Pins | 6 | V |
| $T_S$ | Storage Temperature | 165 | °C |
| $T_J$ | Junction Operating Temperature | -40 to 150 | °C |

## ESD and Surge Ratings

| Symbol | Description | Value | Units |
|---|---|---|---|
| $V_{ESD\_HBM}$ | JEDEC-JS-001 Human Body Model (HBM)[4] | 2 | kV |
| $V_{ESD\_CDM}$ | JESD22-C101, Charged device model (CDM), All pins | 0.5 | kV |
| $V_{ESD\_CD}$ | IEC 61000-4-2 Contact Discharge[5] | 8 | kV |
| $V_{ESD\_AGD}$ | IEC 61000-4-2 Air-Gap Discharge[5] | 15 | kV |

## Thermal Capabilities[6]

| Symbol | Description | Value | Units |
|---|---|---|---|
| $\Theta_{JA}$ | Thermal Resistance – Junction to Ambient | 30.27 | °C/W |
| $P_D$ | Maximum Power Dissipation | 3.30 | W |
| $\Delta P_D/\Delta T$ | Derating Factor Above $T_A$ = 25°C | -33 | mW/°C |

## Recommended Operating Conditions[7]

| Symbol | Parameter | Min. | Typ.[8] | Max. | Units |
|---|---|---|---|---|---|
| $V_{IN\text{-}AF\ (Type\ 1\ PD)}$ | Input Power Supply | 42.5 | 48 | 57 | V |
| $V_{IN\text{-}AT\ (Type\ 2\ PD)}$ | | 42.5 | 48 | 57 | V |
| $V_{IN\text{-}BT\ (Type\ 3\ PD)}$ | | 42.5 | 48 | 57 | V |
| $V_{IN\text{-}BT\ (Type\ 4\ PD)}$ | | 41.1 | 48 | 57 | V |
| $V_{IN\text{-}LP}$ | Local Power Mode (VOUT and GND)[9] | 9.5 | | 57 | V |
| $T_A$ | Ambient Operating Temperature Range | -40 | | +85 | °C |
| $T_{J\_MAX}$ | Recommended Maximum Junction Operating Temperature | -40 | | 125 | °C |

2. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
3. Steady state or transient conditions like system start-up and other noise conditions. Device must not be exposed to sustained over-voltage condition at this level. See section on Rectification and Protection for further details on Integrated Surge Protection.
4. Human Body Model and Charged Device Model ESD limits are specified at the chip level.
5. Air Discharge, and Contact Discharge are specified at the system level.
6. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
7. The recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Kinetic does not recommend exceeding them or designing to Absolute Maximum Rating.
8. Typical specification, not 100% tested. Performance guaranteed by design and/or other correlation methods.
9. Power transformer must be capable of handling the full voltage range.

## Electrical Characteristics[10]

Unless otherwise noted, specifications are for $T_J$ = -40°C to +125°C. Typical specifications are for $T_J$ = +25°C and $V_{IN}$ = 48V (at RJ45 Input). Typical specifications not 100% tested.

### PD (All PD Voltage Limits Specified at the RJ45 Interface)

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{INRUSH\_AF}$ | Inrush Current Limit (AF) – Type 1 PD | For VOUT ≤ 16V during startup, $C_{IN}$ = 5µF (Total System input) | 50 | 160 | 240 | mA |
| $I_{INRUSH\_AT}$ | Inrush Current Limit (AT) – Type 2 PD | For VOUT ≤ 16V during startup, $C_{IN}$ = 5µF (Total System input) | 210 | 320 | 400 | mA |
| $I_{INRUSH\_BT}$ | Inrush Current Limit (BT) – Type 3 PD | For VOUT ≤ 16V during startup, $C_{IN}$ = 10µF (SINGLE-SIGNATURE) | 300 | 410 | 500 | mA |
| $I_{INRUSH\_BT2}$ | Inrush Current Limit (BT) – Type 4 PD | For VOUT ≤ 16V during startup, $C_{IN}$ = 20µF (SINGLE-SIGNATURE) | 380 | 500 | 600 | mA |
| $I_{IN\_AF}$ | Operating Current – Type 1 | RCURR = GND, device configured for 13W operation | | | 450 | mA |
| $I_{IN\_AT}$ | Operating Current – Type 2 | RCURR =5kΩ, device configured for 30W operation | | | 800 | mA |
| $I_{IN\_BT1}$ | Operating Current – Type 3 | RCURR =10kΩ, device configured for 60W operation | | | 1500 | mA |
| $I_{IN\_BT2}$ | Operating Current – Type 4 | RCURR = left open, device configured for 90W operation | | | 2300 | mA |
| $I_{LIM\text{-}AF}$ | PoE Current Limit – Type 1 | RCURR = GND, device configured for 13W operation | 450 | 600 | | mA |
| $I_{LIM\text{-}AT}$ | PoE Current Limit – Type 2 | RCURR =5kΩ, device configured for 30W operation | 800 | 1000 | | mA |
| $I_{LIM\text{-}BT1}$ | Operating Current – Type 3 | RCURR =10kΩ, device configured for 60W operation | 1500 | 1800 | | mA |
| $I_{LIM\text{-}BT2}$ | Operating Current – Type 4 | RCURR = left open, device configured for 90W operation | 2300 | 2700 | | mA |
| $R_{DS\text{-}ON}$ | Hot-Swap FET On Resistance | $I_{IN}$ = 2A | | 0.1 | 0.2 | Ω |
| $V_{DET\_MIN}$ | Min Detection Signature voltage | | | | 2.7 | V |
| $V_{DET\_MAX}$ | Max Detection Signature voltage | | 10.1 | 12.5 | 14.5 | V |
| $V_{CL\_LOW}$ | Classification Lower Threshold | | 11.0 | 12.5 | 14.5 | V |
| $V_{CL\_HIGH}$ | Classification Upper Threshold | | 20.5 | 22.0 | 25 | V |
| $V_{MARK\_MIN}$ | Min Mark Event Voltage | | | | 6.9 | V |
| $V_{MARK\_MAX}$ | Max Mark Event Voltage | | 10.0 | 12.5 | 13.0 | V |
| $V_{CLMK\_HYS}$ | Classification-Mark Hysteresis | | | 1.5 | | V |
| $V_{CL\_RST}$ | Classification Reset Voltage | | 2.81 | | 6.90 | V |
| $I_{CLASS\_}$ | Classification Current: signature 0 | For Voltage classification range: 12.5< $V_{CL}$<20.5 | 1 | | 4 | mA |
| | Classification Current: signature 1 | | 9 | | 12 | mA |
| | Classification Current: signature 2 | | 17 | | 20 | mA |
| | Classification Current: signature 3 | | 26 | | 30 | mA |
| | Classification Current: signature 4 | | 36 | | 44 | mA |
| $V_{IN\_UVLO\_R}$ | Input UVLO Threshold | $V_{IN}$ Rising | 37 | 38 | 42 | V |
| $V_{IN\_UVLO\_F}$ | | $V_{IN}$ Falling | 30 | 32 | 34 | V |

(continued next page)

10. KTA1140 is guaranteed to meet performance specifications over the -40°C to +125°C operating temperature range by design, characterization, and correlation with statistical process controls.

## Electrical Characteristics (continued)[11]

Unless otherwise noted, specifications are for $T_J$ = -40°C to +125°C. Typical specifications are for $T_J$ = +25°C and $V_{IN}$ = 48V (at RJ45 Input). Typical specifications not 100% tested.

### VDD5/VBN Internal Regulator

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{VDD5/BN}$ | Output Voltage | $C_{VDD5/VBN}$ =1µF | | 4.7 | | V |

### Detection

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $R_{DET}$ | Detection Resistance | | 24.3 | 25.5 | 26.0 | KΩ |
| $V_{DOF}$ | Detection offset voltage (for the IC only) | | | | 0.6 | V |

### Maintain Power Signature (MPS)

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $I_{MPS}$ | MPS Current Threshold | The Current is measured on Vout | | 35 | | mA |
| $R_{AMPS}$ | Resistance options on AMPS pin to GND to program the MPS current amplitude. | $R_{AMPS}$=237kΩ | | 10 | | mA |
| | | $R_{AMPS}$=150kΩ | | 16 | | mA |
| | | $R_{AMPS}$=118kΩ | | 20 | | mA |

### Local Power Mode

| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $V_{LV}$ | LVMODE Threshold LOW | | | 1.2 | 1.3 | V |
| $V_{HV}$ | LVMODE Threshold HIGH | | 1.6 | 1.7 | | V |

### Thermal Protection

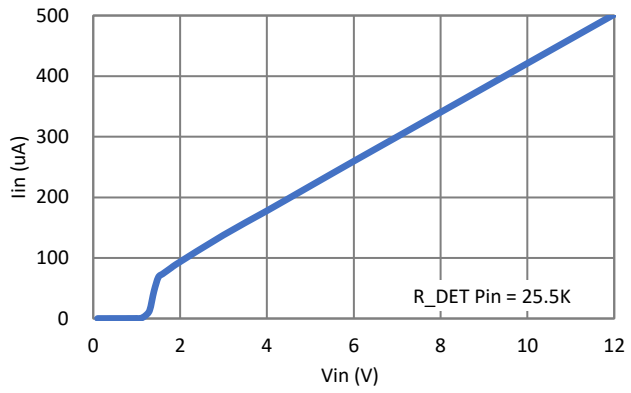
| Symbol | Description | Conditions | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| $T_{J\_TS}$ | Thermal Shutdown Temperature | | | 160 | | °C |
| $T_{J\_HYS}$ | Thermal Shutdown Hysteresis | | | 30 | | °C |

11. Device is guaranteed to meet performance specifications over the -40°C to +125°C operating temperature range by design, characterization, and correlation with statistical process controls.

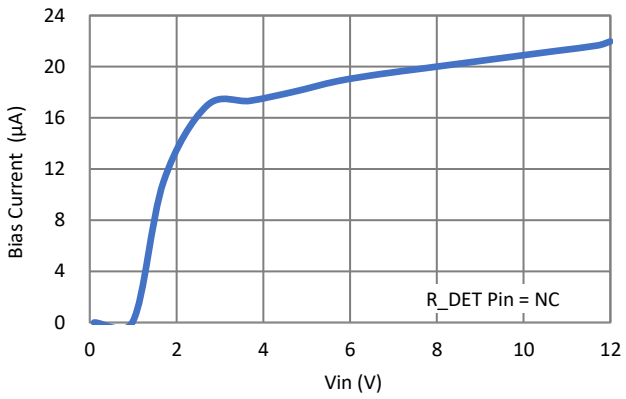
## Typical Characteristics

$V_{IN}$ = 48V, Downstream DC-DC Vo = 12V, Io = 6A, $T_A$ = 25°C, unless otherwise specified.

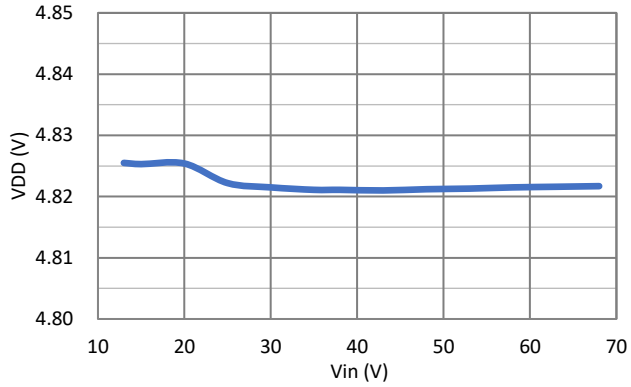
**Detection Current vs. Input Voltage**



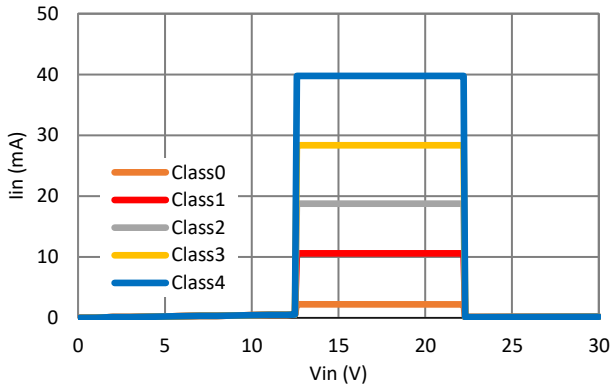

**Detection Current vs. Input Voltage**



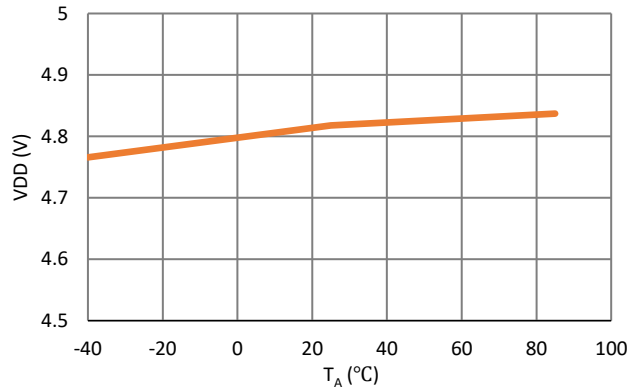

**VDD vs. Vin**



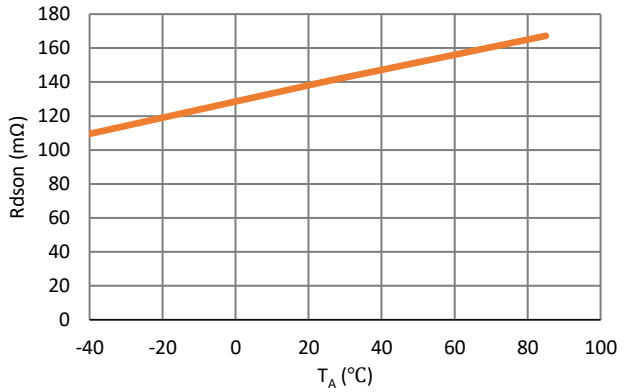

**Classification Current vs Input Voltage**




**VDD vs. Temperature**




**RDSON vs. Temperature**

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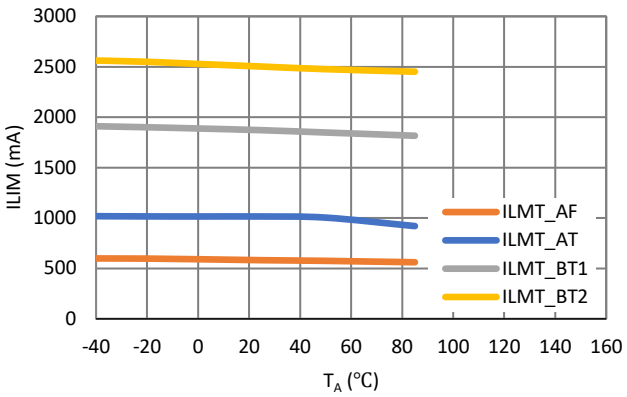
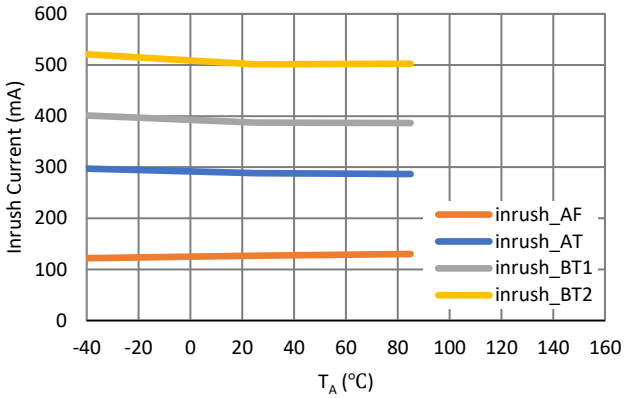
## Typical Characteristics (continued)

$V_{IN}$ = 48V, Downstream DC-DC Vo = 12V, Io = 6A, $T_A$ = 25°C, unless otherwise specified.

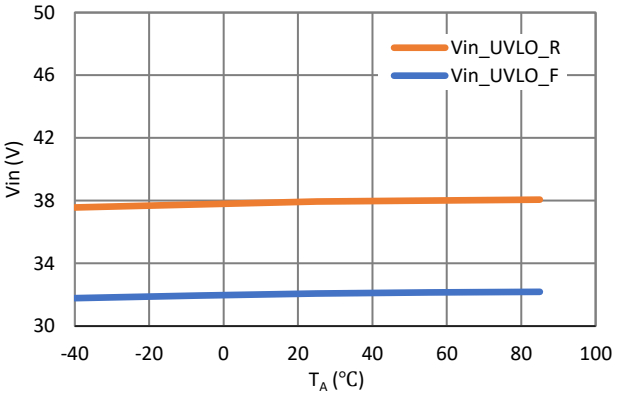
**ILIM vs. Temperature**



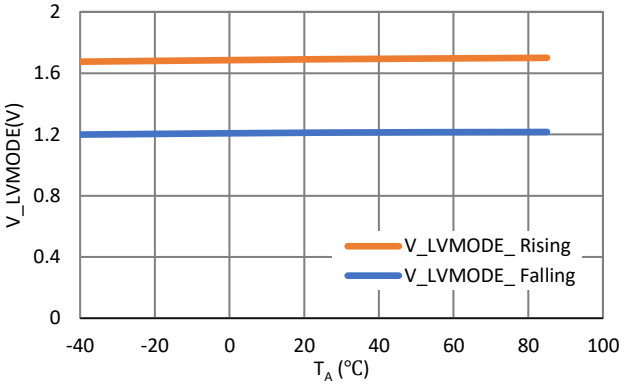

**Inrush Current vs Temperature**



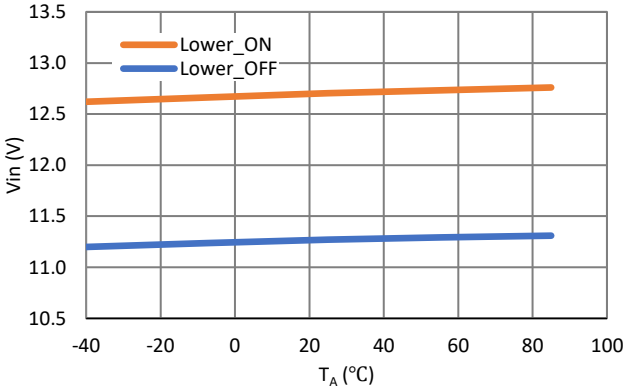

**UVLO vs. Temperature**



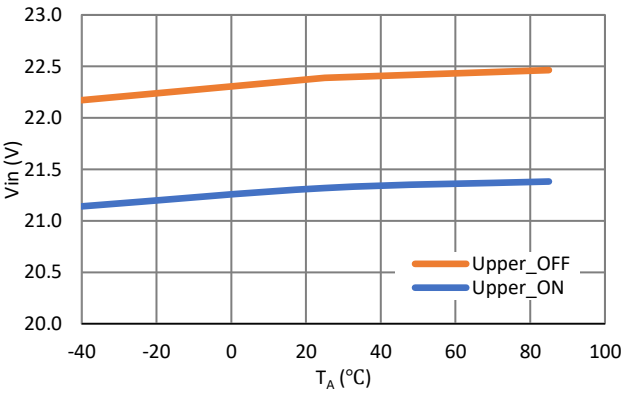

**LVMODE Threshold vs. Temperature**




**Class Lower Threshold vs. Temperature**




**Class Upper Threshold vs. Temperature**

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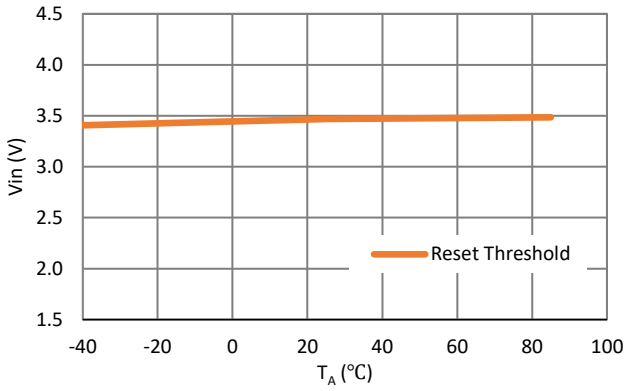
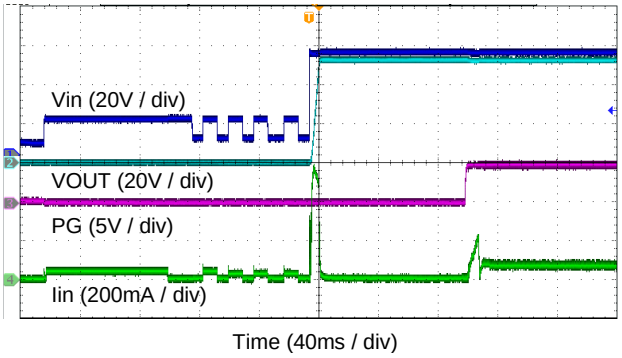
## Typical Characteristics (continued)

$V_{IN}$ = 48V, Downstream DC-DC Vo = 12V, Io = 6A, $T_A$ = 25°C, unless otherwise specified.

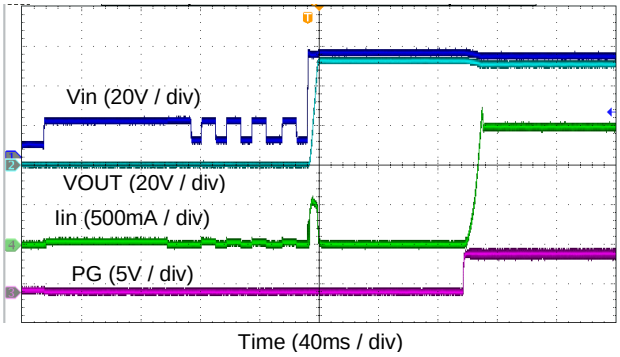
**Mark Reset Threshold Voltage vs. Temperature**



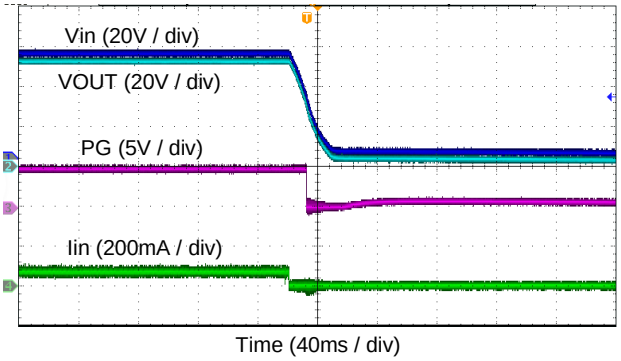

**Startup with PSE Input at Downstream 12V-0A Load**



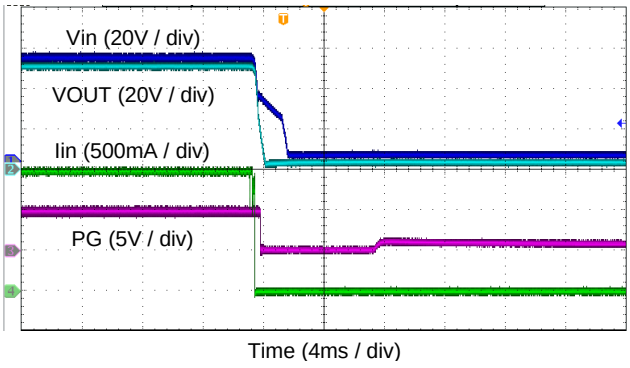

**Startup with PSE Input at Downstream 12V-6A Load**



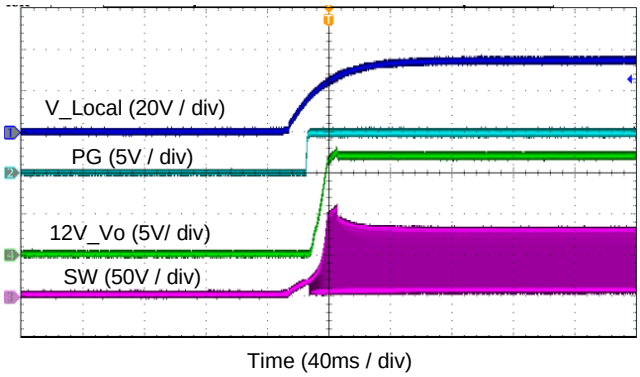

**Shutdown by PSE at Downstream 12V-0A Load**




**Shutdown by PSE at Downstream 12V-6A Load**




**Startup with Local Power at Downstream 12V-0A Load**

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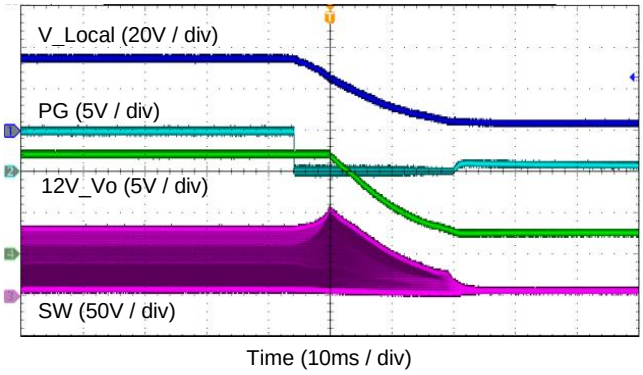
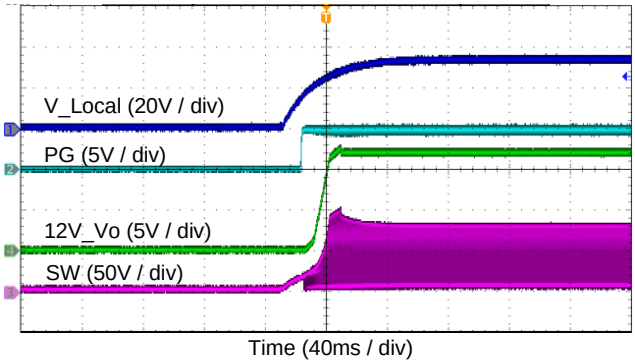
## Typical Characteristics (continued)

$V_{IN}$ = 48V, Downstream DC-DC Vo = 12V, Io = 6A, $T_A$ = 25°C, unless otherwise specified.

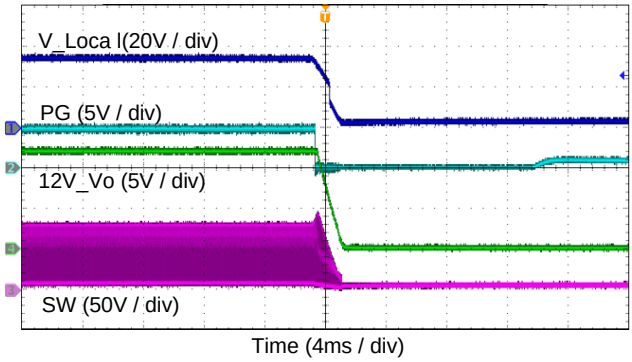
**Shutdown with Local Power at Downstream 12V-0A Load**



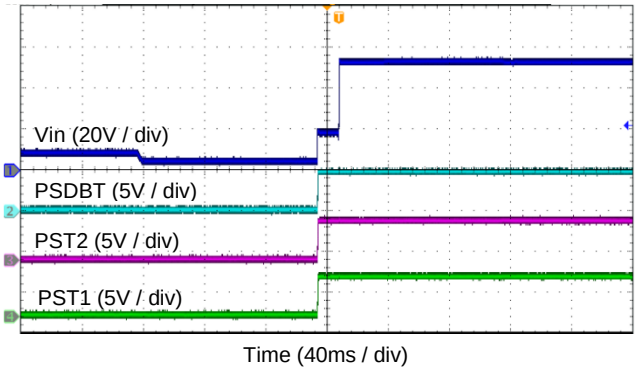

**Startup with Local Power at Downstream 12V-6A Load**



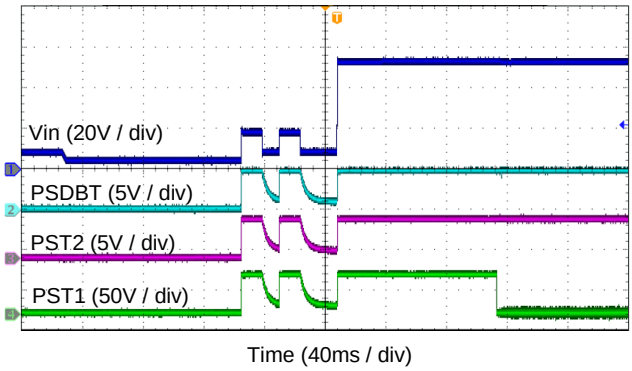

**Shutdown with Local Power at Downstream 12V-6A Load**



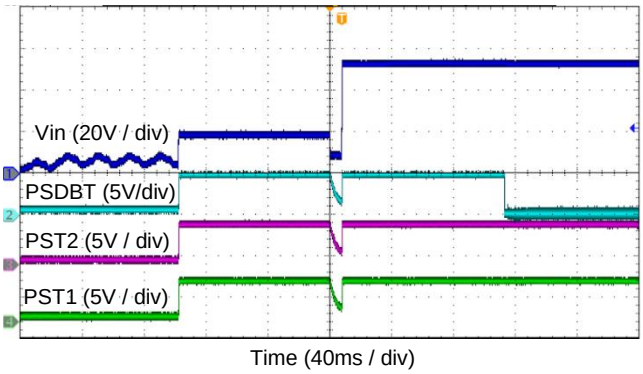

**PoE. BT Detect at PSE12 Class0-3**




**PoE. BT Detect at PSE12 Class4**




**PoE. BT Detect at PSE34 Class0-3**

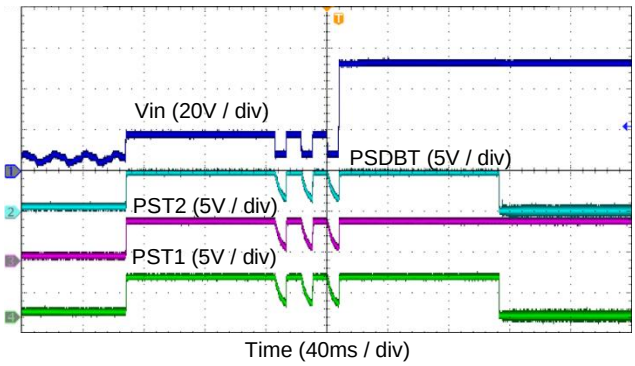



(continued next page)

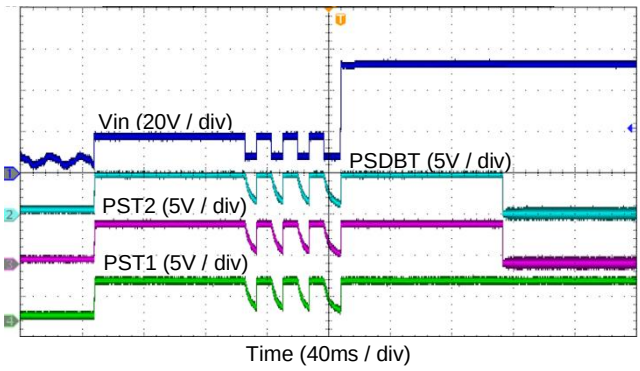
## Typical Characteristics (continued)

$V_{IN}$ = 48V, Downstream DC-DC Vo = 12V, Io = 6A, $T_A$ = 25°C, unless otherwise specified.

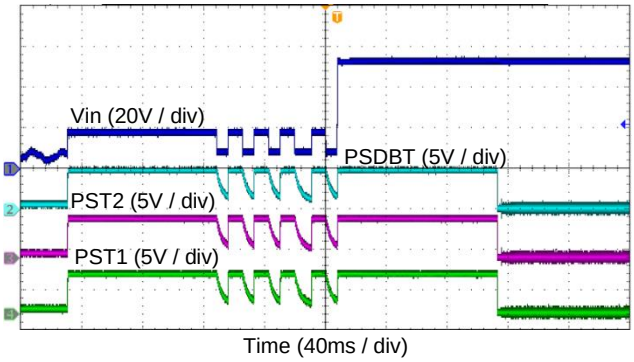
**PoE. BT Detect at PSE34 Class4**



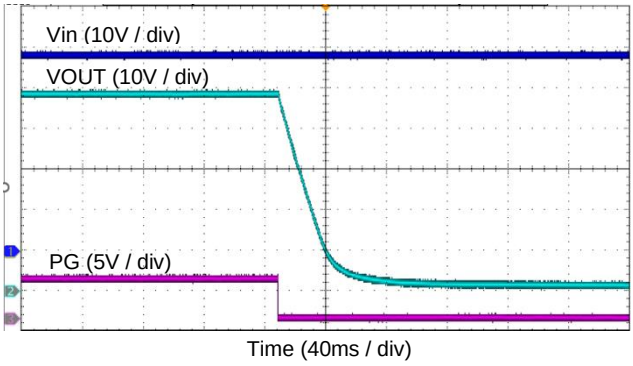

**PoE. BT Detect at PSE34 Class5-6**



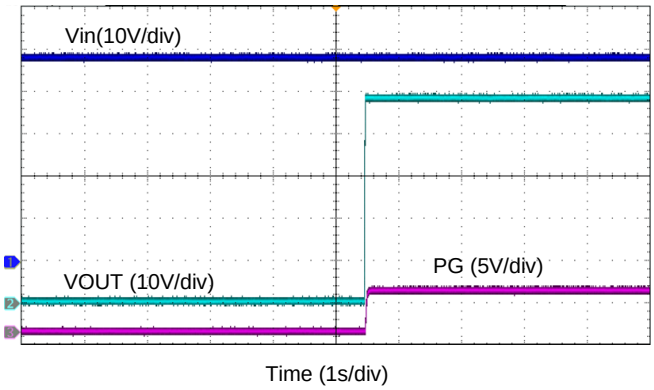

**PoE. BT Detect at PSE34 Class7-8**




**Over Temperature Protection**




**Over Temperature Release**



## Functional Block Diagram

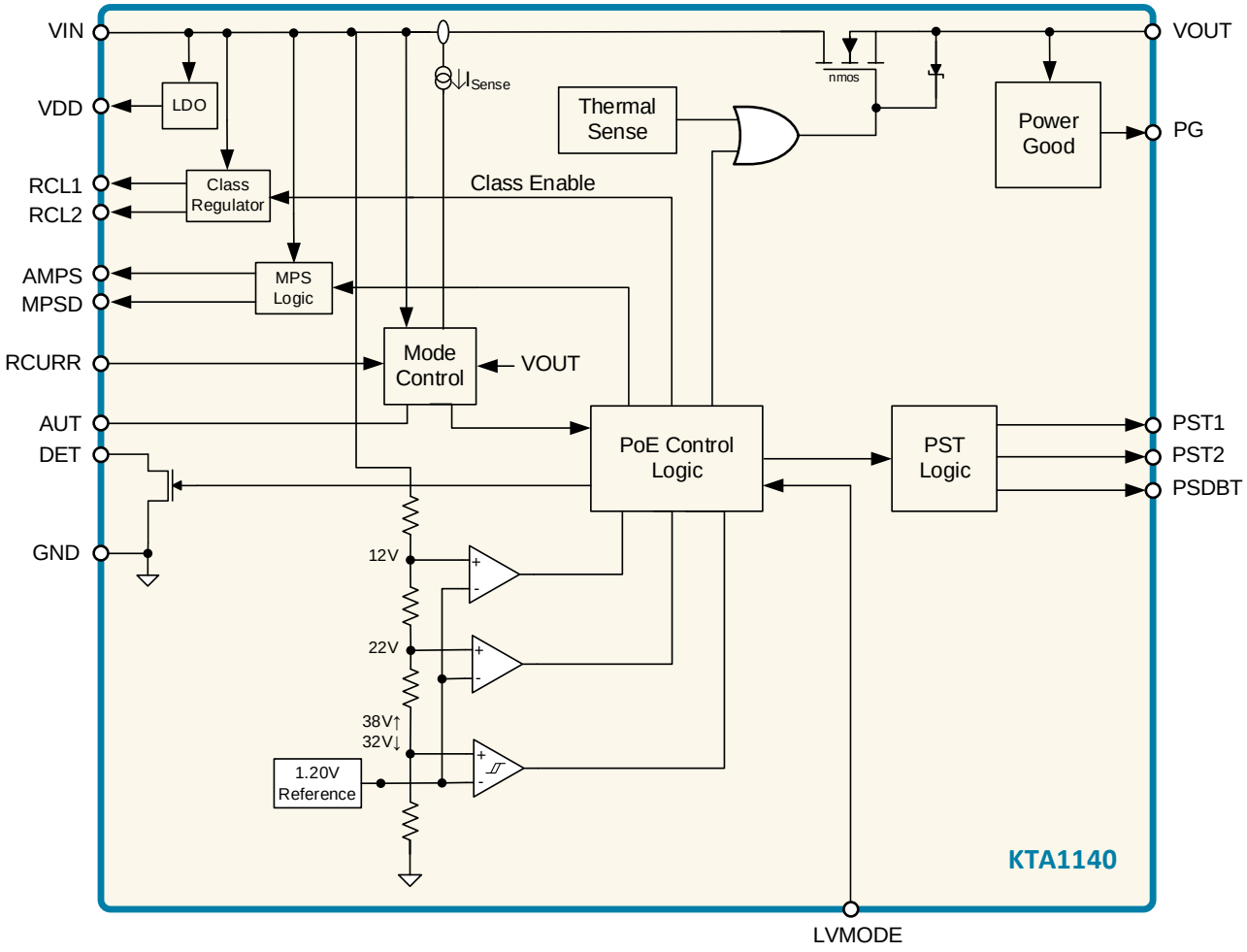



**Figure 1. KTA1140 Block Diagram**

## Functional Description

### Overview of PoE

Power over Ethernet (PoE) offers an economical alternative for powering end network appliances, such as IP telephones, wireless access points, security and web cameras, and other powered devices (PDs). PoE standards IEEE® Std. 802.3af, 802.3at and 802.3bt are intended to unify the delivery method of usable power over Ethernet cables to remotely powered client devices. These standards define a method for detecting and querying PDs and then supplying a range of current levels based on the power class the device belongs to. By employing this method, designers can create systems that predict and minimize power usage, allowing the maximum number of devices to be supported on a powered Ethernet network.

The power source that provides current through the Ethernet cables to remote devices is referred to as the Power Sourcing Equipment (PSE). The powered device (PD) on the other end of the Ethernet cable negotiates for and

receives the agreed-upon power. IEEE® Std. 802.3af limits PSE power delivery to <13W at the PD input (Type 1 PD). IEEE® 802.3at allows for >13W power levels and up to <25.5W (Type 2 PD). There two higher power levels in IEEE® 802.3bt limit PSE power delivery to <51W (Type 3 PD) and <71.3 (Type 4 PD) at the PD input.

**Table 1. Classification Settings for PoE Power Device**

| PD Requested Class | Standard | PD Power (Watt) | PSE Power (Watt) | PD Type | MAX Number of Events | 2 or 4 Pair Power | Auto Class |
|---|---|---|---|---|---|---|---|
| 0 | 802.3af | 12.95 | 15.4 | 1 | - | 2 or 4 Pair | NO |
| 1 | 802.3af | 3.84 | 4 | 1 | 1 | 2 Pair Only | NO |
| 2 | 802.3af | 6.49 | 7 | 1 | 1 | 2 Pair Only | NO |
| 3 | 802.3af | 12.95 | 15.4 | 1 | 1 | 2 or 4 Pair | NO |
| 4 | 802.3at | 25.5 | 30 | 2 | 2 | 2 or 4 Pair | NO |
| 5 | 802.3bt | 38.25 | 45 | 3 | 4 | 4 Pair Mandatory | Optional |
| 6 | 802.3bt | 51 | 60 | 3 | 4 | 4 Pair Mandatory | Optional |
| 7 | 802.3bt | 62 | 75 | 4 | 5 | 4 Pair Mandatory | Optional |
| 8 | 802.3bt | 71.3 | 90 | 4 | 5 | 4 Pair Mandatory | Optional |

The PSE uses the following sequence to detect a connected PD, determine how much power it requires and then initiate supply current to the device:

- **Reset** — Power is withdrawn from the PD if the applied voltage falls below a specified level.
- **Signature Detection** — The PSE detects and evaluates whether the PD is a valid PoE device.
- **Classification** — The PSE reads the power requirement of the PD. The Classification level identifies how much power the PD will require from the Ethernet line. This permits optimum use of the total power available from the PSE.
- **On** — Operational state, during which the PSE provides the allocated power level to the PD.

This sequence occurs as a progressively rising voltage level from the PSE. It is designed to prevent high voltages from being present on an Ethernet line that does not have a valid PD attached (for user and non-PoE device safety).

To design PoE systems according to IEEE® standards, the following constraints apply listed in Table 2:

**Table 2. PoE Requirements**

| Requirement | Value |
|---|---|
| Input voltage at Type 1 PD interface | 37V-57V |
| Input voltage at Type 2 PD interface | 42.5V-57V |
| Input voltage at Type 3 PD interface | 42.5V-57V |
| Input voltage at Type 4 PD interface | 41.1V-57V |
| Output voltage from Type 1 PSE | 44-57V |
| Output voltage from Type 2 PSE | 50-57V |
| Output voltage from Type 3 PSE | 50-57V |
| Output voltage from Type 4 PSE | 52-57V |
| Minimum operating current limit, Type 1 @ PSE min output voltage | 350mA |
| Minimum operating current limit, Type 2 @ PSE min output voltage | 600mA |
| Minimum operating current limit, Type 3 @ PSE min output voltage | 600 mA per pair |
| Minimum operating current limit, Type 4 @ PSE min output voltage | 960 mA per pair |

## KTA1140 Details Overview

The KTA1140 is a fully integrated PD that provides the functionality required for Power-over-Ethernet (PoE) applications. The optimized architecture reduces external component cost in a small footprint while delivering high performance.

To meet PoE standards requirements, the KTA1140 is a fully integrated PoE PD controller for Type1-4 PD implementations. The KTA1140 meets all system requirements for the IEEE® 802.3 standard for Ethernet and all power management requirements for IEEE® standard 802.3bt-2018.

The KTA1140 acts as an interface to the PSE, performing all detection, classification, and inrush current limiting control necessary for compliance with the PoE standards. An internal MOSFET and control circuit limits the inrush and steady-state current drawn from the Ethernet line. External rectification bridges protect against polarity reversal, to provide alternative detection.

The KTA1140 also passes the 8kV Contact Discharge and 15kV Air Discharge requirements, tested per IEC 61000-4-2. EMI compliance of KTA1140-based designs has been verified for CISP22 and FCC Class-B radiated and conducted emissions.

## Rectification and Protection

To protect against polarity reversal, an external Rectification bridge is required. In conjunction with the external bridge, the KTA1140 provides over-voltage and transient protection on the line side of the Hot-Swap FET.

The KTA1140 is implemented in a robust 100V process technology. By integrating robust input protection circuitry, Kinetic has produced a solution that provides much faster response to surge events. The design also limits stray surge current from passing through sensitive circuits, such as the Ethernet PHY device and enables low-impedance safe discharge paths directly to earth ground. The protection circuit has been carefully designed to ensure that during these surge events, where currents can reach as high as 30A, voltages do not exceed critical breakdown and spark gap limits, protecting the PD from damage by the event. This enables system designers to achieve 15kV/8kV Air/Contact Discharge system ESD performance.

## PD Controller

The KTA1140 PD Control Interface is designed to provide full PD functionality for IEEE® 802.3af/at/bt compliant systems, with programmable support for standard PD control functions.

The PD Controller provides the following major functions:

- A resistance/capacitance connection path for the detection signature.
- Classification current for power classification.
- Type 4 (Class 8) Power capability for PD supply
- Power management and thermal protection override, including UVLO (Under Voltage Lock Out).
- PSE type indicator output signal pins
- PSDBT Output pin when connected to a PSE.BT that can deliver more than 30Watts.
- 5-Event Physical Layer classification.

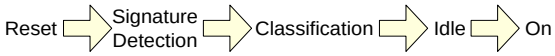
## Modes of Operation

The KTA1140 has five operating modes:

1. **Reset** — all blocks are disabled.
2. **Detection** — the external PD detection signature resistance / capacitance components are applied across the input.
3. **Classification** — PD indicates power requirements to the PSE via different number of Events Classification for IEEE® 802.3af/at/bt
4. **Idle** — this state is entered after Classification and remains until full-power input voltage is applied.

5. **On** — The PD is enabled and supplies power to the DC-DC controller and the local application circuitry.

As the supply voltage from the PSE increases from 0V, the KTA1140 transitions through the modes of operation in this sequence:




If no PSE or local power supply is present, line voltage will be zero, which will hold the KTA1140 in the Reset state. The KTA1140 does not affect the Ethernet link function.

### Reset

When the voltage supplied to the KTA1140 drops below the minimum valid detection voltage (i.e. <2.7V), the chip will enter the Reset state. While in Reset, the power supply to the PD is disconnected, the KTA1140 consumes very little power and the device reverts to the pre-detection status.

### Detection Mode

During the detection sequence, the PSE periodically applies a voltage to the PD to read its detection signature. The reading of the signature determines if a PD is present.

During detection, the PSE applies two sequential voltages, 1V or more apart, within the detection voltage range of 2.7V to 10.1V. It extracts a detection signature resistance value from the incremental I-V slope. Valid I-V slope resistance values are between 23.75kΩ and 26.25kΩ.

With the KTA1140, detection signature resistance is generated by an external resistor connected between VIN and GND on DET Pin. Typically this is a 25.5kΩ, 1% resistor. With this value of RSIGNATURE, the PSE normally detects a total effective signature resistance of approximately 25kΩ, which is within the 802.3af/at/bt specification range of 23.75kΩ to 26.25kΩ.

Valid PD detection also requires a valid detection signature capacitance of 0.05µ to 0.12µF at 2.7 to 10.1V, and 1.9V maximum offset voltage, per the IEEE® 802.3bt standard, measured at the PD input connector. KTA1140 detection signature capacitance is generated by an external 68nF capacitor connected between VIN and GND. The offset voltage is mainly provided by the external bridge voltage drop.

### Classification Mode

Each class represents a power allocation range for a PD to assist the PSE in managing power distribution. IEEE® Std. 802.3bt defines classes of power levels for PDs, listed in Table 1. The KTA1140 supports IEEE® Std. 802.3af/at and IEEE® Std. 802.3bt up to 5-Event Physical Layer classification, as shown in Figure 2 and Figure 3. The KTA1140 identifies the PSE as Type 1 to Type 4. If the 4 or 5 Event method is detected by the PD controller during the classification stage, it asserts the PSDBT low level output indicates availability of higher system power in BT level for Class 5 to 8. If the PD controller detects 1 to 3 classification events, it identifies the PSE to be not BT level and the PSDBT pin is asserted high.

In real applications, noise or transient ringing on the line during classification phase can lead to false classification events or PSE type detection. To prevent such false positives, the KTA1140 integrates a proprietary digital filter to filter out noise events as long as 100uS during the classification phase, ensuring a very reliable BT Detection.

KTA1140 allows the user to program the classification current via external resistors. Each of the two external resistors connected between RCL1 and RCL2 pins and ground provide a distinct classification signature to the PSE, and are used to define the power class requested by the PD.

The current drawn by each resistor, combined with the internal circuit and leakage create the classification signature current. The number of classification cycles then determines how much power is allocated by the PSE.

The current, power levels and programming resistor values for each class are shown in Table 3. For Class 0, the pin needs to be pulled up to VDD pin. This can be a direct short to VDD or using a resistor up to 100kΩ.

Use the following equation to determine the typical classification current:

$$I_{Class}\,[mA] = 2.0 + \frac{2360}{R_{Class}[k\Omega]} \qquad (1)$$

Tolerance = Maximum of ±1.8mA or ±9%

Once the classification process is done, the PD removes the classification current to conserve power.

**Table 3. Classification Settings Resistors Selection in RCL1 and RCL2 Pins**

| PD Class | PD Type | Power (W) | Class 1 Signature | Class 2 Signature | Number of Class Events for Max Power | $R_{CL1}$ (kΩ), 1% | $R_{CL2}$ (kΩ), 1% |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 0.44-12.95 | 0 | 0 | 1 | Pull-up (0-100kΩ) to VDD pin | Pull-up (0-100kΩ) to VDD pin |
| 1 | 1 | 0.44-3.84 | 1 | 1 | 1 | 280 | 280 |
| 2 | 1 | 3.84-6.49 | 2 | 2 | 1 | 143 | 143 |
| 3 | 1 | 6.49-12.95 | 3 | 3 | 1 | 90.9 | 90.9 |
| 4 | 2 | 12.96-25.5 | 4 | 4 | 2,3 | 63.4 | 63.4 |
| 5 | 3 | 25.5-38.25 | 4 | 0 | 4 | 63.4 | Pull-up (0-100kΩ) to VDD pin |
| 6 | 3 | 38.25-51 | 4 | 1 | 4 | 63.4 | 280 |
| 7 | 4 | 51-62 | 4 | 2 | 5 | 63.4 | 143 |
| 8 | 4 | 62-71.3 | 4 | 3 | 5 | 63.4 | 90.9 |

### Idle Mode

After the classification process, the PD enters Idle mode while it waits for On-state power delivery from the PSE. PD Current usage is limited to monitoring circuitry to detect the On-state voltage threshold.

### On State

In the On state, the KTA1140 is supplying power across the Ethernet line(s) to the PD. Then, the PD turns on and full power is available via the KTA1140 to the DC-DC converter and the systems.

### PoE Power-On Startup Waveform

Figure 2 represents the power-on sequence for PoE operation for af and at power level . Figure 3 represents the higher power level up to 5 classification events power-on sequence for PoE.bt operation. These waveforms reflect typical voltages present at the PD during signature, classification and power-on.

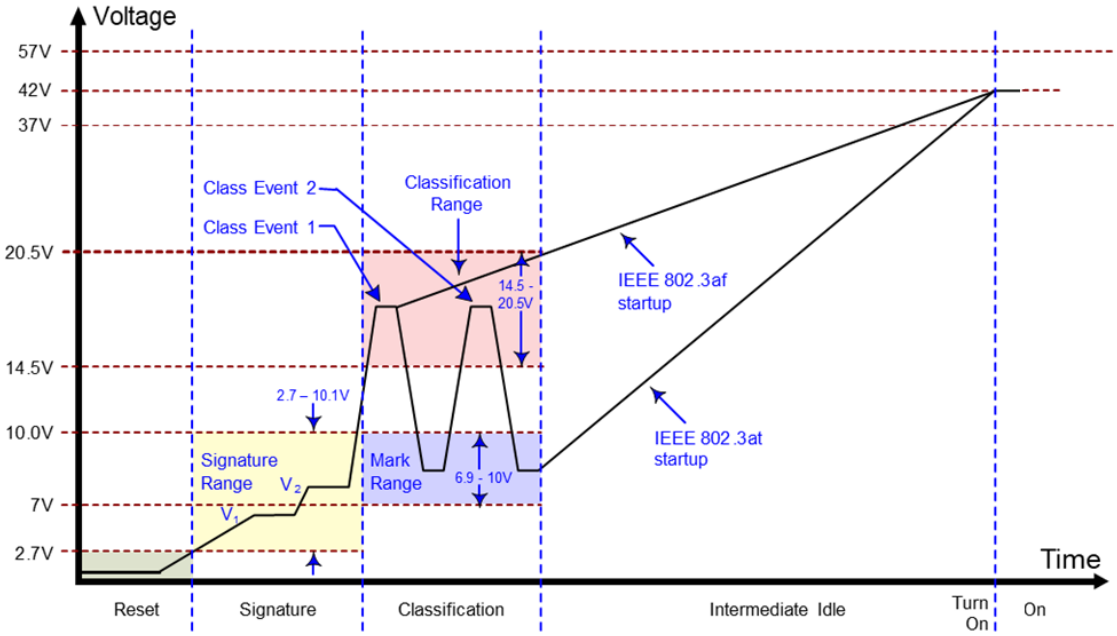



**Figure 2. IEEE 802.3af/at Typical Power-On Waveform**

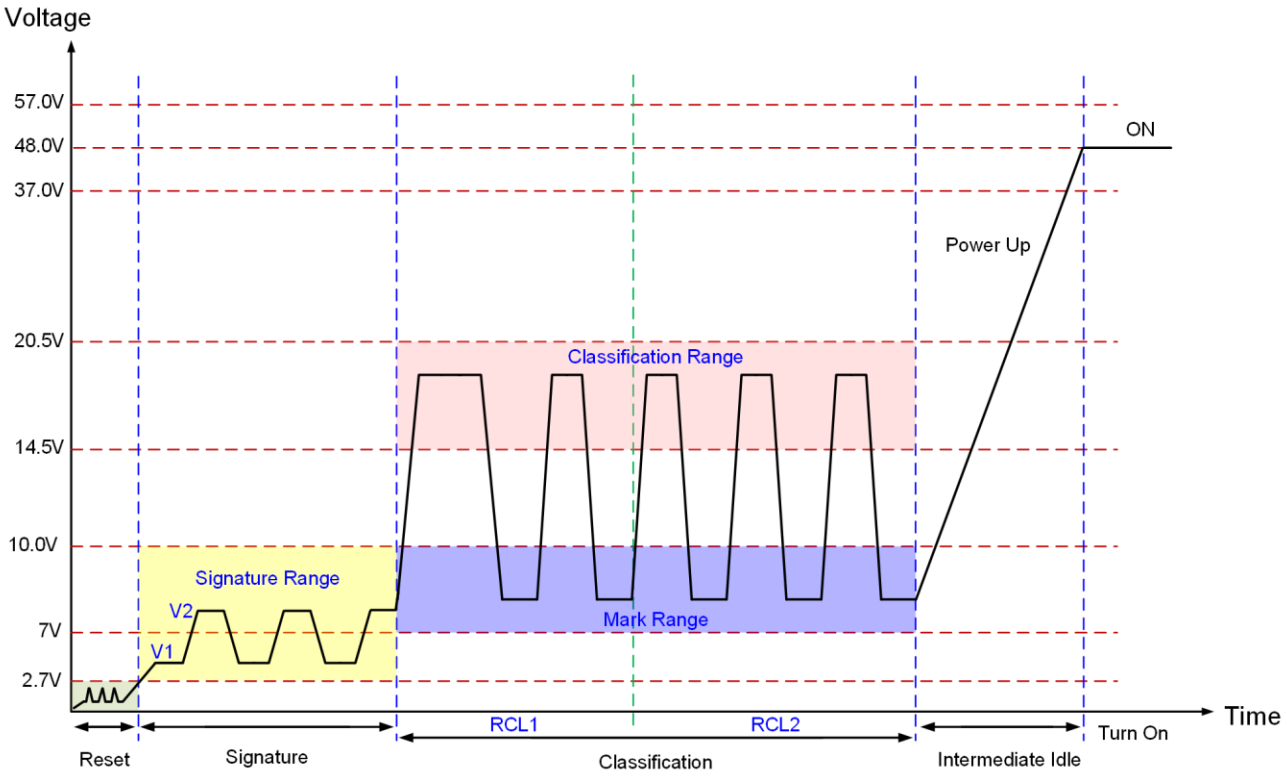



**Figure 3. IEEE 802.3bt Typical Power-On Waveform**

1. Voltages V1 and V2 with minimum 1V differences are applied by the PSE to extract a signature value.
2. The PSE takes current/impedance readings during Class/Mark Events to determine the class of the PD. At this time, the PD presents a load current determined by the resistances connected to the RCLASS pins (RCL1 and RCL2)
3. After the PSE measures the PD load current, if it is a high-power PSE, it presents a mark voltage (6.9-10V), followed by a second classification voltage (14.5-20.5V). The PD responds by presenting a load current as determined by RCL1 and RCL2. After the PSE measures the PD load current the second time and determines that is can deliver the requested power, it moves into the On state by raising the voltage to approximately 48V in PoE.BT power levels.

### PST1, PST2 and PSDBT Pins

PST1 and PST2 are Open Drain active-low output pins that indicate PSE type and power level. For PoE.BT power level, PSDBT output pin provides an indicator when Type 3 or 4 PSE is detected.

The PSDBT pin will be set low once the PD recognizes the completion of the 4 or 5 Event Physical Layer Classification, as initiated by a Type 3 or 4 PSE and completion of PG set to high that takes typically 100ms after Vout power up. The pin will remain low and will only be reset high by the occurrence of a Reset or a power-down event. PSDBT pin remains high if it identifies the PSE partner to be Type 1 or 2 during the Classification phase.

The state of PST1, PST2 and PSDBT is used to provide information relative to the PSE Type (1-2 or 3-4) and its allocated power. Table 4 lists the encoding corresponding to various combinations of PSE Type, PD Class and allocated power.

Demotion conditions also correspond to cases where the PSE allocated power is lower than what the PD is requesting. The allocated power is determined by the number of classification cycles having been received. KTA1140 power demotion details and PST1, PST2 and PSDBT status are provided in Table 5.

**Table 4. KTA1140 Power LEVEL Details based on PST1, PST2 and PSDBT Pins Status**

| PSE Type | PD Class | # Class Events | PSE Power LEVEL | PST1 | PST2 | PSDBT |
|---|---|---|---|---|---|---|
| 1 or 2 | 0 | 1 | 12.95 | High | High | High |
| 1 or 2 | 1 | 1 | 3.84 | High | High | High |
| 1 or 2 | 2 | 1 | 6.49 | High | High | High |
| 1 or 2 | 3 | 1 | 12.95 | High | High | High |
| 2 | 4 | 2 | 25.5 | Low | High | High |
| 3 or 4 | 0 | 1 | 12.95 | High | High | Low |
| 3 or 4 | 1 | 1 | 3.84 | High | High | Low |
| 3 or 4 | 2 | 1 | 6.49 | High | High | Low |
| 3 or 4 | 3 | 1 | 12.95 | High | High | Low |
| 3 or 4 | 4 | 2 or 3 | 25.5 | Low | High | Low |
| 3 or 4 | 5 | 4 | 38.25 | High | Low | Low |
| 3 or 4 | 6 | 4 | 51 | High | Low | Low |
| 4 | 7 | 5 | 62 | Low | Low | Low |
| 4 | 8 | 5 | 71.3 | Low | Low | Low |

**Table 5. KTA1140 Power Demotion Details**

| PSE Type | PD Class | # Class Events | PSE Power LEVEL | PST1 | PST2 | PSDBT |
|---|---|---|---|---|---|---|
| 1 or 2 | 0 | 1 | 12.95 | High | High | High |
| 1 or 2 | 1 | 1 | 3.84 | High | High | High |
| 1 or 2 | 2 | 1 | 6.49 | High | High | High |

## Local Power Mode (LVMODE)

The LVMODE pin can be used in applications where the PD appliance is designed to draw power from either the Ethernet cable or an external DC local power adapter. The LVMODE pin is a voltage mode input pin with low and high thresholds as defined in the electrical characteristics for the PD. The LVMODE is asserted when the input exceeds the high threshold ~1.7V, and is de-asserted when the input voltage is below the low threshold ~1.2V threshold. If LVMODE operation is not desired, the LVMODE pin should be connected to GND.

Figure 4 shows a simplified internal implementation and external application circuit required to use the LVMODE feature. When power is applied at the local adapter input, the KTA1140 enters Local Voltage Mode. This opens the internal Hot-Swap FET switch while the DC-DC converter is in operation.

In this configuration, local power always takes priority, even in presence of PoE power, irrespective of their relative voltages. If local power is removed, the device will exit Local Voltage Mode operation and PoE power will be used, if available.

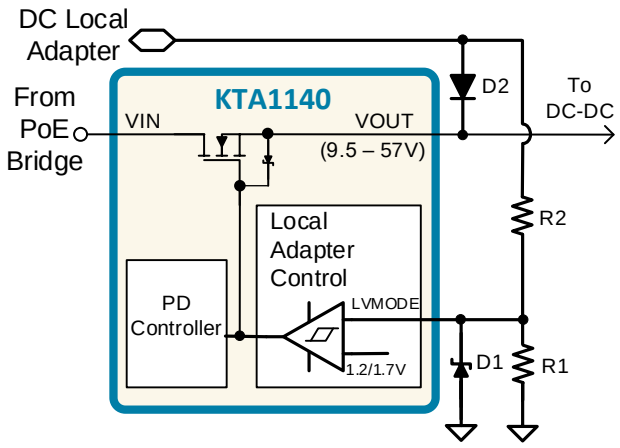



**Figure 4. LVMODE Implementation**

Local power is inserted at the VOUT node through an external diode (D2). Use of a low reverse-leakage diode is recommended. This ensures that when there is no local power, PoE voltage at the VOUT node will not falsely pull up the LVMODE pin due to high reverse leakage through the diode.

An appropriate ratio of R2 and R1 resistors should be used to ensure proper operation across all supply voltages. Though a common value of R2 and R1 can be used across the whole range of local supply voltages from 9.5V to 57V, using different value pairs, will minimize power consumption. The maximum input voltage at the LVMODE pin should not exceed 6V, so a Zener diode (D1) is recommended to limit transient voltage excursions at the pin.

Since the input voltage at the LVMODE pin defines its state, it is not recommended to drive other circuits or components directly from the LVMODE node (such as an LED) that might draw current and voltage changes. LEDs or current-absorbing components may be driven directly from the Local Supply pin.

**Table 6. LVMODE Configuration**

| Local Voltage Range | Recommended Local Adapters |
|---|---|
| 9.5V-57V | 12V, 18V |
| 20V-57V | 24V, 30V |
| 32.4V-57V | 36V, 48V |

### PD Controller Power and Thermal Protection

The KTA1140 provides the following PD controller power and thermal protection:

- Under Voltage Lock Out (UVLO)
- Inrush Current Limit with integrated current sense
- Thermal Limit / Protection

### Under Voltage Lock Out (UVLO)

The KTA1140 contains line Under-Voltage Lock Out (UVLO) circuitry to determine when to power on the PD. If the PSE supply voltage at PD PI is equal or greater than UVLO VIN_RISING, the KTA1140 PD will power on and run; if the PSE supply voltage at PD PI drops below UVLO VIN_FALLING, the KTA1140 PD will power off. The PD circuit controls power flow to the DC-DC controller, to protect the PD from erratic operation or damage.

### Inrush Current Limit / Current Sense

Inrush limiting maintains the cable voltage above the turn-off threshold as the input capacitor charges. This also prevents the PSE from going into current limit mode. The Current Limit/Current Sense circuitry also minimizes the PD on-chip temperature peaks by limiting both inrush and operating current.

During the PD startup sequence, VDS across the Hot-Swap FET is momentarily high as the VOUT output capacitance is charged up. During this state, the Hot-Swap FET experiences a high instantaneous power drop and heating. Therefore, it is recommended that during this startup sequence, the incoming current should only be utilized for the charging of the VOUT node, to minimize the startup time and associated power drop across the FET. There is 108ms default time period for inrush. Also, there is a debounce time of 512µs for OCP.

### Thermal Limit / Protection

The KTA1140 provides thermal protection for itself by monitoring die temperature and reducing maximum current or disconnecting power as needed to prevent its pre-set thermal limits from being exceeded. Thermal current is implemented and disables the Hot swap MOSFET switch above 165˚C. Normal current limits in both cases are re-applied when the die temperature returns below 125˚C.

### Maintain Power Signature and AMPS

To have PSE connected to PD controller a minimum amount of current is needed. This is referred to as the Maintain Power Signature (MPS). Depending on the PD assigned Class and PD signature configuration. To maintain PSE power in situation of very low current, the KTA1140 generates a pulsed current to reaches the required threshold to maintain the power. The pulsed current amplitude and period are automatically selected according to PSE Type (1-2, 3-4), to maintain PSE power while minimizing power consumption.

Table 7 shows the details for MPSD pin to select the MPS duty cycle select driven by a precision current source with voltage limited to less than ~5.5V.

**Table 7. Maintain Power Signature Duty Cycle Selection Details**

| PSE Type | MPSD Pin Resistance Value | Duty Cycle | Ton | Toff |
|---|---|---|---|---|
| 1, 2 | - | - | 88ms | 224ms |
| 3, 4 | GND | 12.5% | 20ms | 140ms |
| 3, 4 | 60.4kΩ | 8.1% | 16ms | 184ms |
| 3, 4 | Open | 5.4% | 12ms | 210ms |

Automatic Maintain Power Signature (AMPS) control can be assigned by AMPS pin with a resistor and appropriate power rating to support the MPS current.

### Auto-Class

Auto-Class is a classification mechanism that allows a PD to communicate its effective maximum power consumption to the PSE. This happens in such a way that the PSE will be able to set the power budget to the effective maximum PD power. This new feature was introduced in the IEEE802.3bt standard to allow a more efficient use of the available power since only the effectively used power needs to be budgeted. A Type 3 or Type 4 PD may optionally support Auto-Class whereas a Type 3 or Type 4 PSE may make use of it to optimize its power management.

A PSE implementing Auto-Class uses the first-class event to inquire if the PD supports Auto-Class, looking for the class current to fall to class 0 current level. If it is the case, the PSE can then proceed to Auto-Class measurement immediately after power up, the PD being required to draw its highest power throughout the bounded period using sliding time window to calculate the power.

### PGOOD Specs Details

Open-Drain, Power-Good Indicator Output pin will be low during detection, classification; 100ms is the typical period (can be trimmed) after power up before PG set to high, until the internal isolation MOSFET in KTA1140 is fully turned on. That will keep the downstream DC-DC converter disabled during inrush. 8 cycle blanking time (can be trimmed or disabled) before pulling down the PG in the case Vout is lower than the defined range. MPS is enabled after PG is high and PG remains high to enable downstream DC-DC converter in MPS mode.

### Startup Sequences

The internal PoE UVLO (Undervoltage Lock Out) circuit holds the Hot-Swap switch off before the PSE provides full voltage to the PD. This prevents the downstream converter circuits from loading the PoE input during detection and classification.

The PSE drives the primary voltage to the operating range once it has decided to power up the PD. When VDD rises above the UVLO turn-on threshold (approximately 38V), KTA1140 enables the Hot-Swap MOSFET with inrush current limit.

The PG pin is in low state; Also the output voltage to DC/DC Controller is also turned off during that time, providing no low supply voltage to the PWM controller, to avoid additional loading that could prevent successful PD and subsequent converter start up. PD current limit is valid after inrush stage(100ms).

### Thermal De-Rating and Board Layout Considerations

The KTA1140 is capable of operating to an industrial temperature range of 85°C in ambient air and up to 125°C junction temperature, without forced cooling. A thermal pad on the underside of the package dissipates the heat generated by the PD die.

In higher power applications in PoE.bt level, designers must consider thermal dissipation as an integral part of their system architecture and plan to remove heat via this pad.

If the PCB landing pattern is properly designed, the QFN package should exhibit a thermal resistance of ΘJA ≈ 30°C/W. For adequate heat dissipation, the board layout must include a ground pad which provides both the ground connection and dissipates the heat energy produced in the chip. Thermal vias are used to draw heat away from the PD package and to transfer it to the backside of the system PCB.

## Applications Circuits

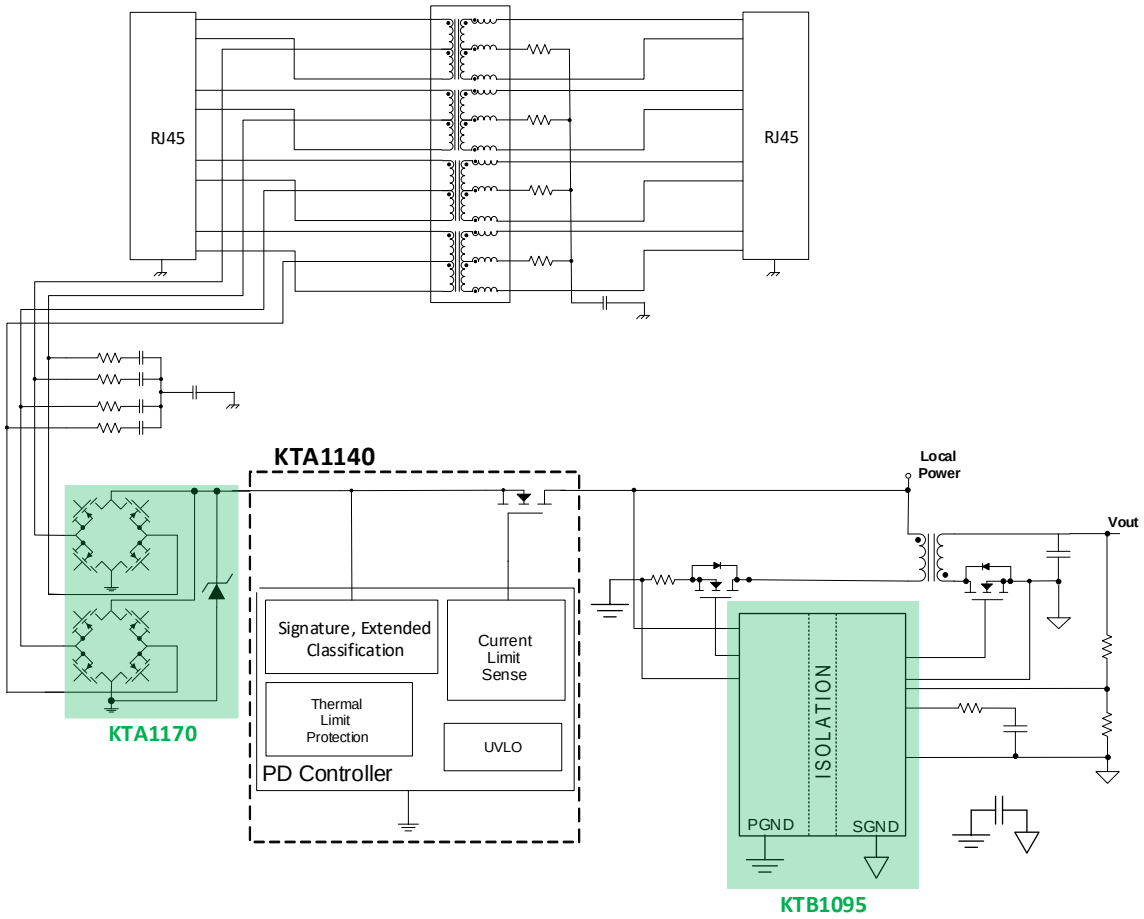



**Figure 5. KTA1140 High-Efficiency Synchronous Flyback DC-DC Solution with Isolated Controller**

Note: This is a simplified conceptual schematic. Please refer to the reference design documentation for detailed design and component information. Full PoE implementation will require two input diode bridges. For simplicity, only one is shown here.

## Applications Circuits (continued)

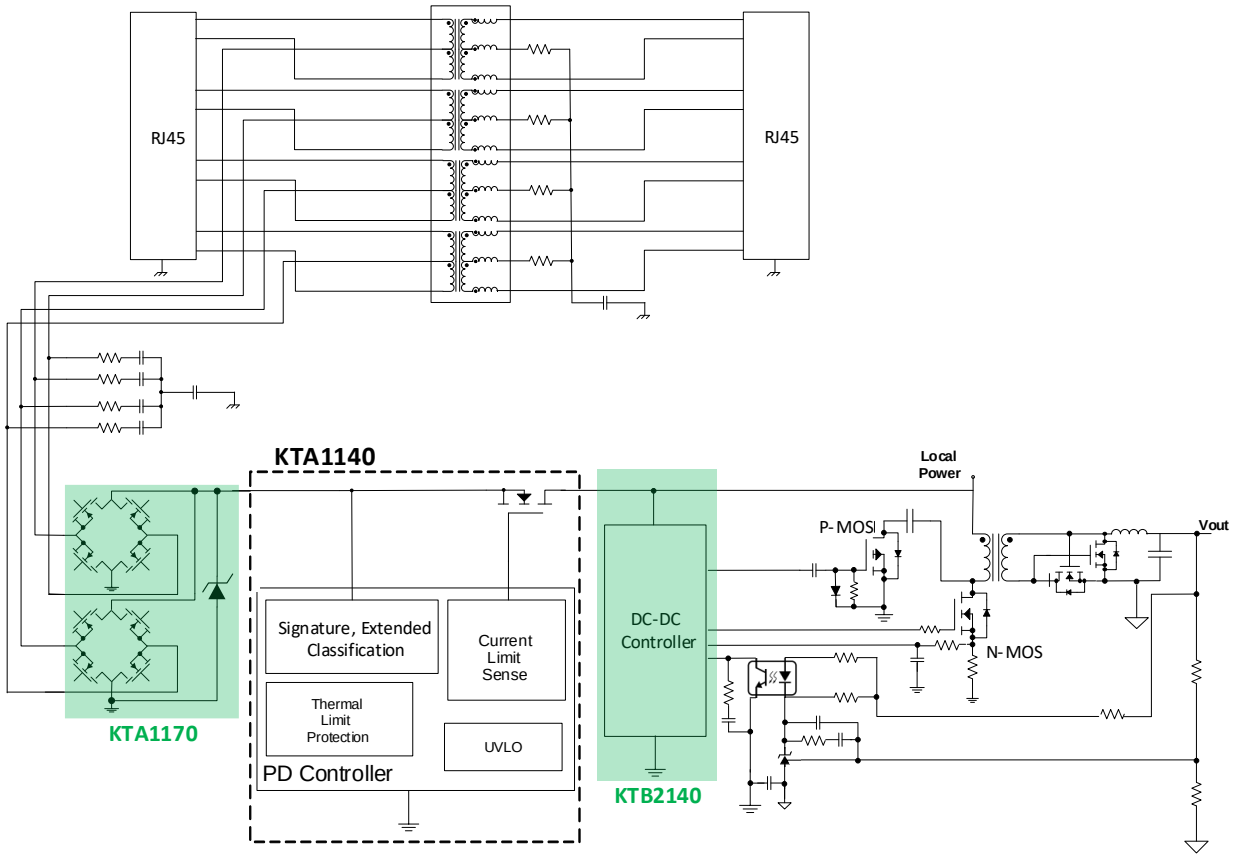
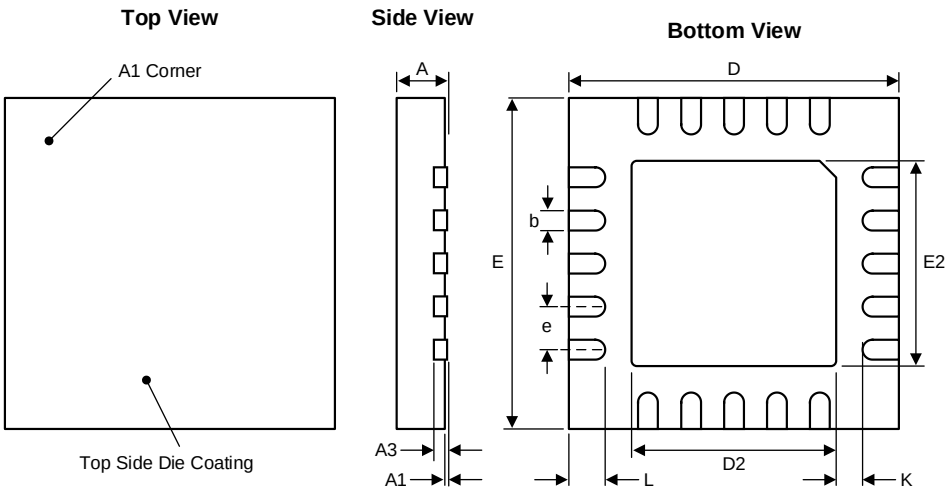



**Figure 6. KTA1140 High-Efficiency Active Clamp Forward Solution for Higher Current Applications**

Note: This is a simplified conceptual schematic. Please refer to the reference design documentation for detailed design and component information. Full PoE implementation will require two input diode bridges. For simplicity, only one is shown here.

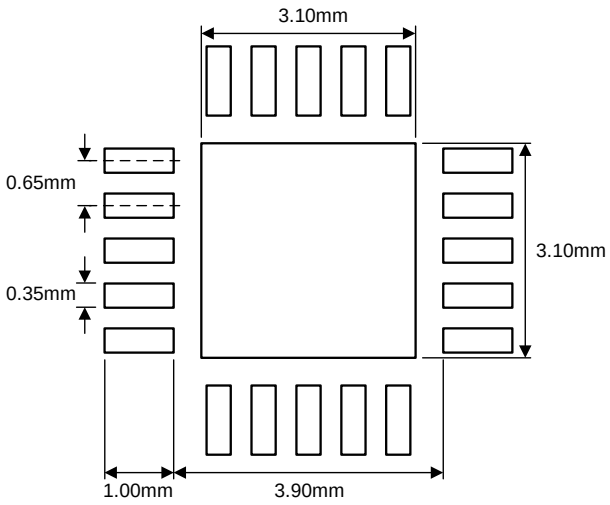
# Packaging Information

## WQFN55-20 (5.00mm x 5.00mm x 0.75mm)




| Dimension | mm | | |
|---|---|---|---|
| | Min. | Typ. | Max. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | 0.200 REF | | |
| b | 0.20 | 0.30 | 0.35 |
| D | 5.00 BSC | | |
| D2 | 3.05 | 3.10 | 3.15 |
| E | 5.00 BSC | | |
| E2 | 3.05 | 3.10 | 3.15 |
| e | 0.65 BSC | | |
| K | 0.20 | 0.40 | – |
| L | 0.45 | 0.55 | 0.65 |

## Recommended Footprint

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