Surge Protected Load Switch with Over-Voltage Protection

Features

- Surge and ESD protected Input
  - Surge Protection
    - IEC 61000-4-5: >100V
  - ESD Protection
    - IEC 61000-4-2 (Level 4)
      - Contact: ±8kV
      - Air Gap: ±15kV
      - Human Body Model ±2kV
- Wide Input voltage range
  - 2.7V to 30V
- Low Quiescent Current 60µA typ.
- N channel MOSFET load switch with low forward voltage drop
  - 140mV @ 1A
- Fast turn-off response time 100ns
- Flexible trip-point options
  - Fixed 6.8V
  - Adj. 4V to 20V
- Auto-enabled switch with typ. 15ms debounce time
- Additional Under voltage (UVLO), Short-circuit and thermal shutdown protection
- Open-drain power good output
- Pb-free WLCSP-9 package
- -40°C to +85°C Temperature Range

Brief Description

The KTS1685 over-voltage protection device features an ultra-low 140mΩ (typical) on-resistance high current integrated MOSFET which actively protects low-voltage systems from voltage supply faults up to +30VDC. An internal clamp protects the device from surges up to 100V.

An input voltage exceeding the over-voltage threshold will cause the internal MOSFET to turn off, preventing excessive voltage from damaging downstream devices.

When the OVLO input set below the external OVLO select voltage, the KTS1685 automatically chooses the internal fixed OVLO threshold, preset to 6.8V (typical). The over-voltage protection threshold can be adjusted with optional resistor divider to a voltage between 4V and 22V.

The device features an open-drain output $\overline{\text{ACOK}}$ indicating a stable supply between the minimum supply voltage and OVLO threshold. In case of fault condition and the device temperature exceeds the maximum junction temperature, the device switches off.

The KTS1685 is available in a RoHS and Green compliant 9-Bump 1.33 x 1.33mm WLCSP.

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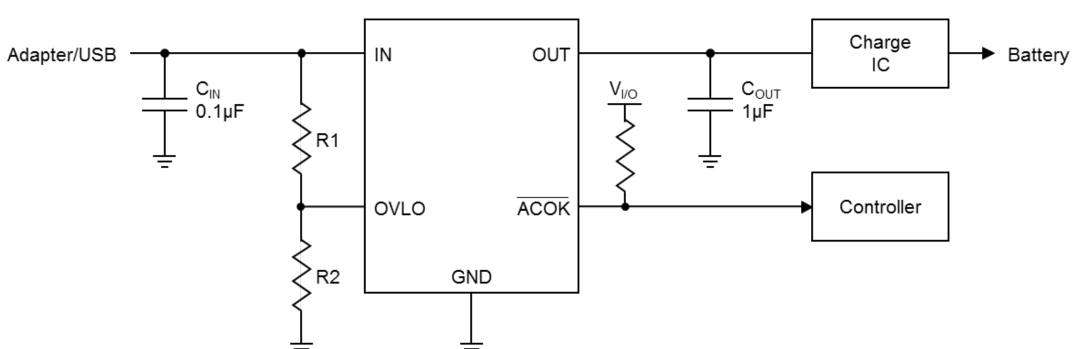
Applications

- Smartphones
- Mobile Internet Devices
- Tablet Computers
- Peripherals

Typical Application



Pin Descriptions

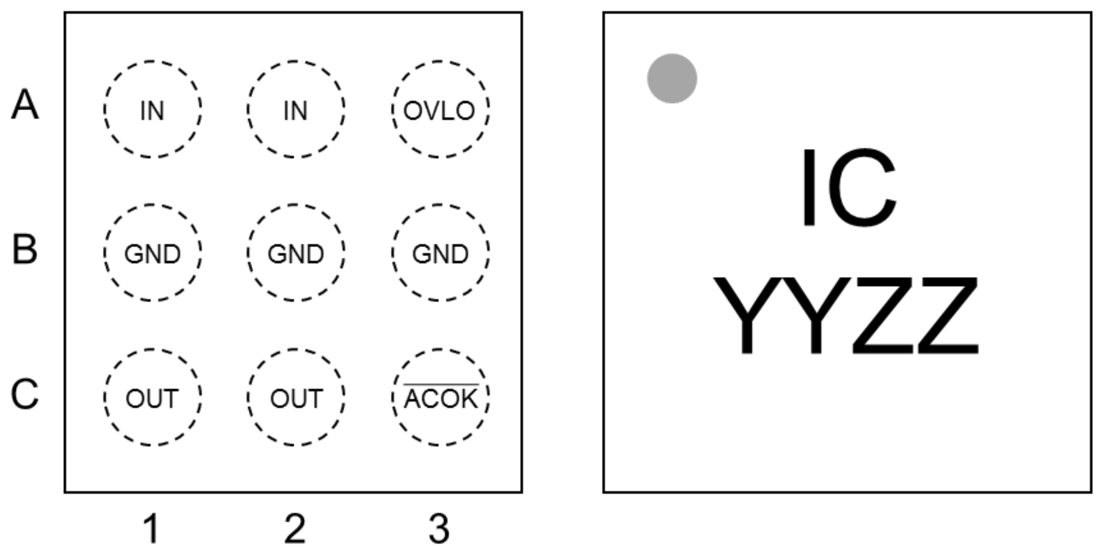
Pin #	Name	Function
A1, A2	IN	Voltage Input. Bypass IN with 0.1µF capacitor as close as possible to the device.
A3	OVLO	External OVLO adjustment. Connect OVLO to GND when using the internal threshold. Connect a resister-divider to OVLO to set a different OVLO threshold.
B1, B2, B3	GND	Ground.
C1, C2	OUT	Output Voltage
C3	$\overline{\text{ACOK}}$	Open-Drain Fault Output. $\overline{\text{ACOK}}$ is pulled high when UVLO or OVLO or OTP condition is present. Connect a pull-up resistor between the logic pin and the system rail.

WLCSP-9

Top View

Top View

TOP VIEW



9-Bump 1.33mm x 1.33mm x 0.6mm
WLCSP Package

YYZZ (Date Code and Assembly Code)
IC = Device Code (Top Mark)

Absolute Maximum Ratings[1]

(T_A = 25°C unless otherwise noted)

Symbol	Description	Value	Units
IN[2]	Input voltage	-0.3 to 30	V
OUT	Output voltage	-0.3 to VIN+0.3	V
OVLO	OVLO Pin	-0.3 to 7	V
$\overline{\text{ACOK}}$	Fault Pin	-0.3 to 6	V
IN, OUT Current	Continuous Current	1.5	A
	Peak Current (10msec)	3.0	A
T_J	Operating Temperature Range	-40 to 150	°C
T_s	Storage Temperature Range	-65 to 150	°C
T_{LEAD}	Maximum Soldering Temperature (at leads, 10 sec)	260	°C

Thermal Capabilities

Symbol	Description	Value	Units
θ_{JA}	Thermal Resistance – Junction to Ambient[3]	100	°C/W
P_D	Maximum Power Dissipation at $T_A \leq 25°C$	1.15	W
$\Delta P_D/\Delta T$	Derating Factor Above T_A = 25°C	-12.8	mW/°C

Recommended Operating Range

Description	Value
Input voltage range	2.7V to 30V
Output capacitance range	Up to 100µF

Ordering Information

Part Number	Marking[4]	Operating Temperature	Package
KTS1685EUE-TR	ICYYZZ	-40°C to +85°C	WLCSP-9

1. Stresses above those listed in Absolute Maximum Ratings may cause permanent damage to the device. Functional operation at conditions other than the operating conditions specified is not implied. Only one Absolute Maximum rating should be applied at any one time.
2. Survives pulse up to 100V with 2Ω series resistance.
3. Junction to Ambient thermal resistance is highly dependent on PCB layout. Values are based on thermal properties of the device when soldered to an EV board.
4. "YYZZ" is the date code and assembly code.

Electrical Characteristics[5]

Unless otherwise noted, the *Min* and *Max* specs are applied over the full operation temperature range of -40°C to +85°C, while *Typ* values are specified at room temperature (25°C). V_{IN} = 5.0V, $I_{IN} \le$ 1.5A

Symbol	Description	Conditions	Min	Typ	Max	Units
INPUT CLAMP						
V_{IN}	Input operating range		2.5		30	V
V_{IN_CLAMP}	Input clamp voltage	I_{IN} = 10mA, T_A = +25℃		32		V
I_{IN}	Input supply current	V_{IN} = 5V, $V_{IN} < V_{OVLO}$			120	µA
V_{IN_UVLO}	Under voltage lockout threshold	V_{IN} rising		2.3		V
V_{UVLO_HYST}	Under voltage lockout hysteresis			0.1		V
OVP						
V_{IN_OVLO}	Internal over voltage trip level	V_{IN} rising	6.6	6.8	7.0	V
$V_{IN\_OVLO\_HYS}$	OVLO Hysteresis	V_{IN} falling		0.2		V
V_{OVLO_TH}	OVLO preset threshold range		1.19	1.21	1.23	V
	Adjustable OVLO threshold range		4		22	V
V_{OVLO_SEL}	External OVLO select threshold		0.2	0.25	0.3	V
$R_{DS(ON)}$	Switch On-Resistance	V_{IN} = 5V, I_{IN} = 1.0A, T_A = +25℃		140	200	mΩ
I_{OVLO}	OVLO input leakage current	$V_{OVLO} = V_{OVLO\_TH}$	-100		100	nA
FAULT						
V_{OL}	$\overline{ACOK}$ output low voltage	$V_{I/O}$ = 3.3V, I_{SINK} = 1mA			0.4	V
$V_{\overline{ACOK}\_LEAK}$	$\overline{ACOK}$ leakage current	$V_{I/O}$ = 3.3V, $\overline{ACOK}$ de-asserted	-1		1	µA
TIMING – Figure 1						
t_{DEB}	Debounce time	Time from 2.5V < $V_{IN} < V_{IN\_OVLO}$ to V_{OUT} = 10% of V_{IN}		15		ms
t_{SS}	Soft-start time	V_{OUT} = 10% of V_{IN} to soft-start off		15		ms
t_{ON}	Switch turn-on time	V_{IN} = 5V, R_L = 100Ω, C_{LOAD} = 100µF V_{OUT} from 10%, V_{IN} to 90% V_{IN}		2		ms
t_{OFF}	Switch turn-off time	$V_{IN} > V_{OVLO}$ to V_{OUT} = 80% of V_{IN}, R_L = 100Ω, V_{IN} rising at 2V/µs		100		ns
ESD PROTECTION (IEC61000-4-2)						
V_{ESD}	Human Body Model(HBM) Model = 2	All pins		±15		kV
	IEC61000-4-2 Contact discharge	IN pin		±8		kV
	IEC61000-4-2 Air gap discharge	IN pin		±15		kV
THERMAL SHUTDOWN						
t_{J-TH}	IC junction thermal shutdown threshold			135		°C
	IC junction thermal shutdown hysteresis			20		°C

5. KTS1685 is guaranteed to meet performance specifications over the –40°C to +85°C operating temperature range by design, characterization and correlation with statistical process controls.

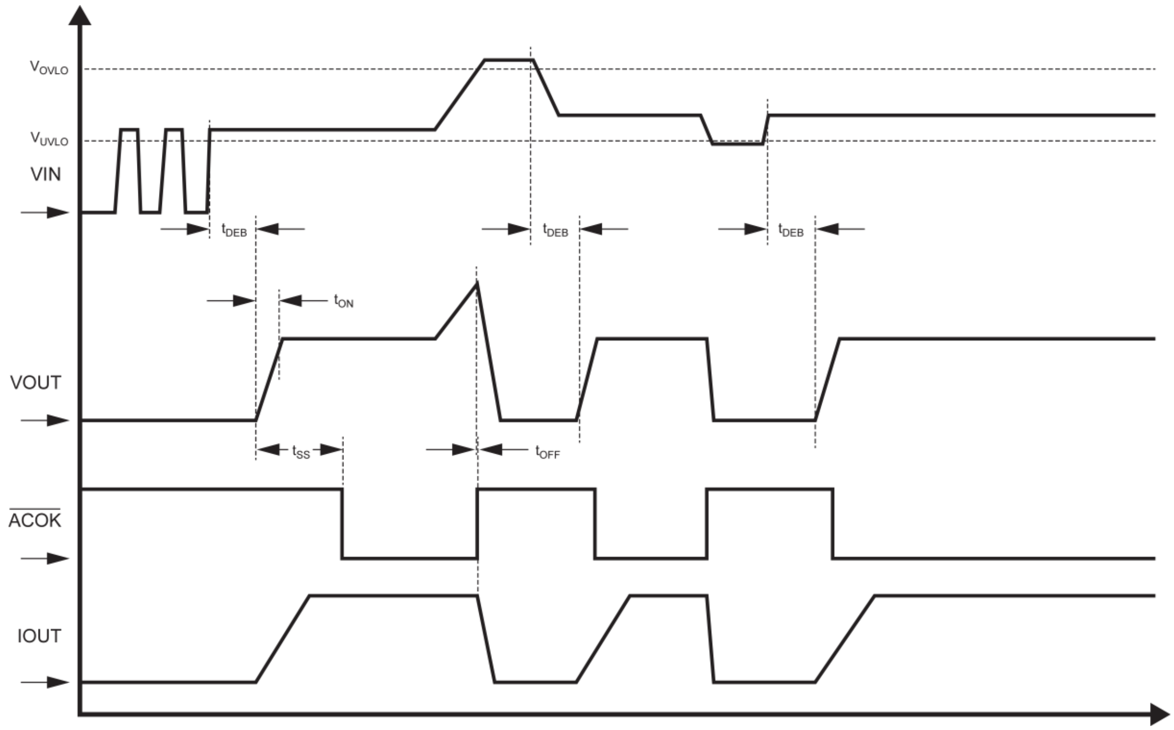
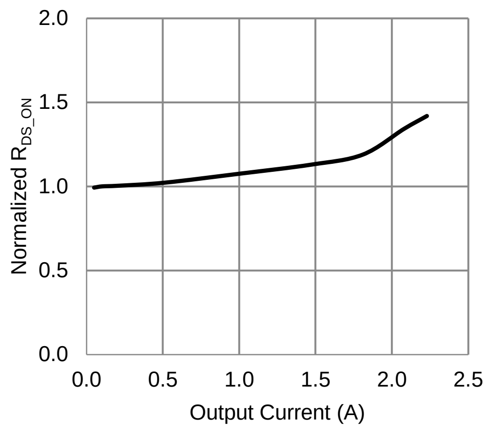


Figure 1. Timing Diagram

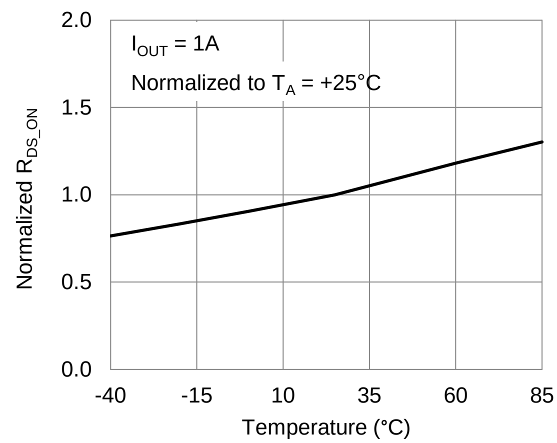
Typical Characteristics

V_{IN} = 5V, C_{IN} = 0.1µF, C_{OUT} = 1µF, OVLO pin = GND, Temp = 25°C unless otherwise specified.

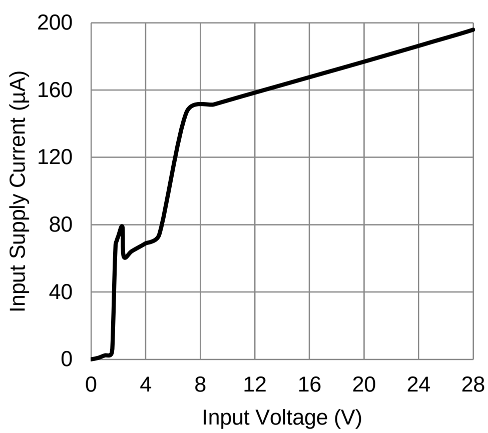
Normalized R_{DSON} vs. Output Current



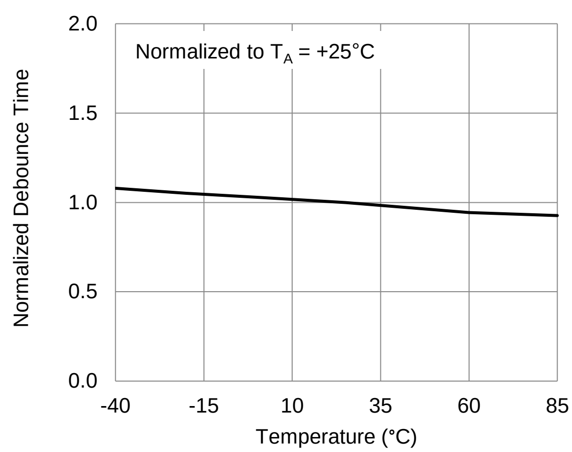
Normalized R_{DSON} vs. Temperature



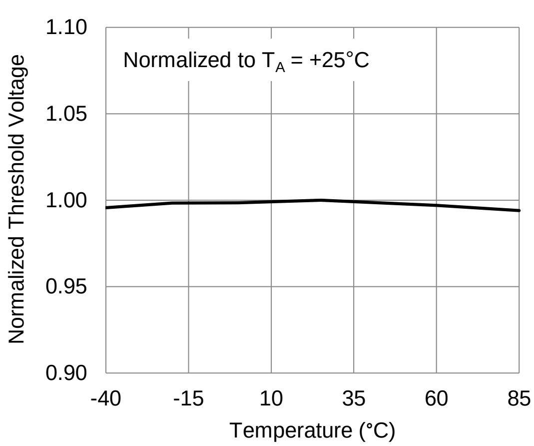
Input Supply Current vs. Input Voltage (no load)



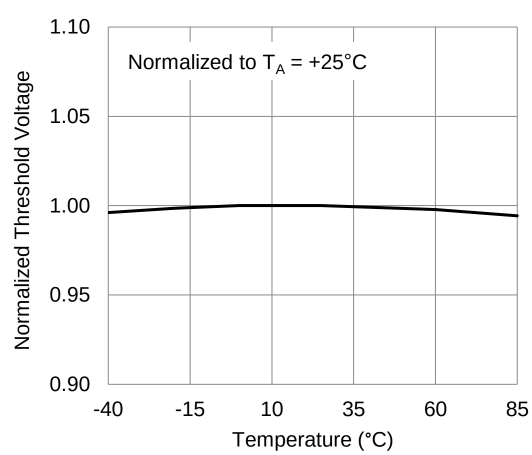
Normalized Debounce Time vs. Temperature



Normalized Fixed OVLO vs. Temperature (OVLO pin GND)



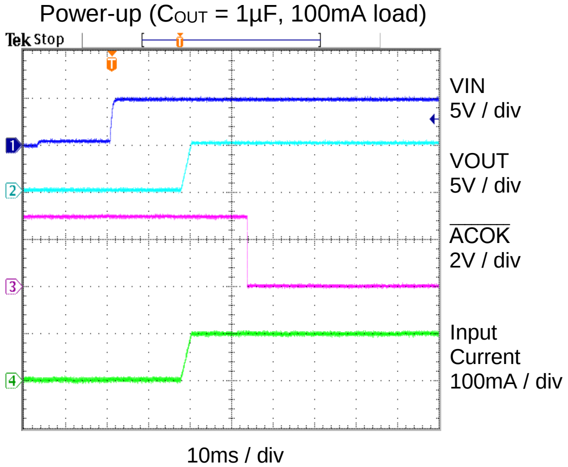
Normalized Adjustable OVLO Threshold vs. Temperature



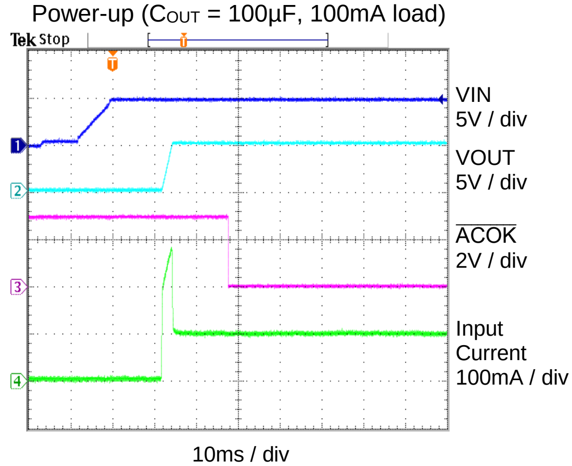
Typical Characteristics (continued)

V_{IN} = 5V, C_{IN} = 0.1µF, C_{OUT} = 1µF, OVLO pin = GND, Temp = 25°C unless otherwise specified.

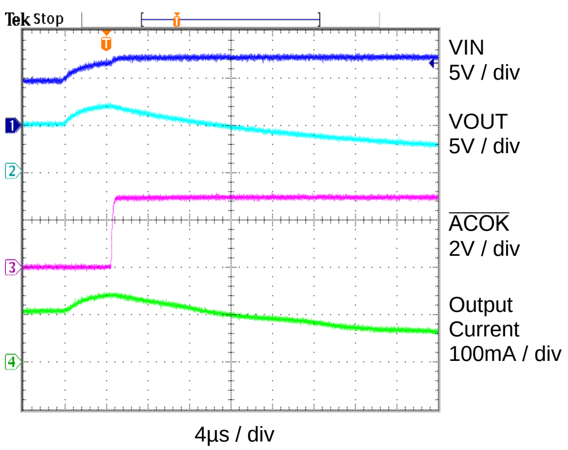
Power-up (C_{OUT} = 1µF, 100mA load)



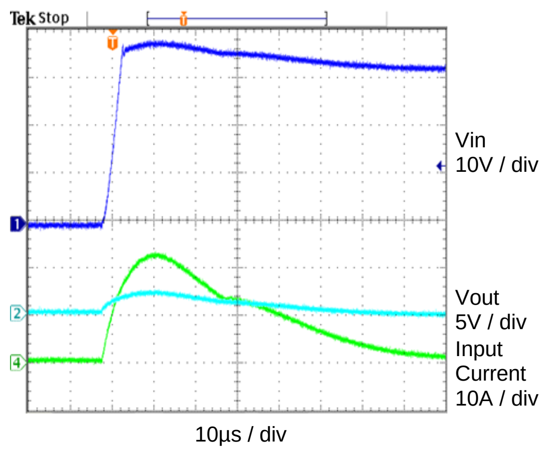
Power-up (C_{OUT} = 100µF, 100mA load)



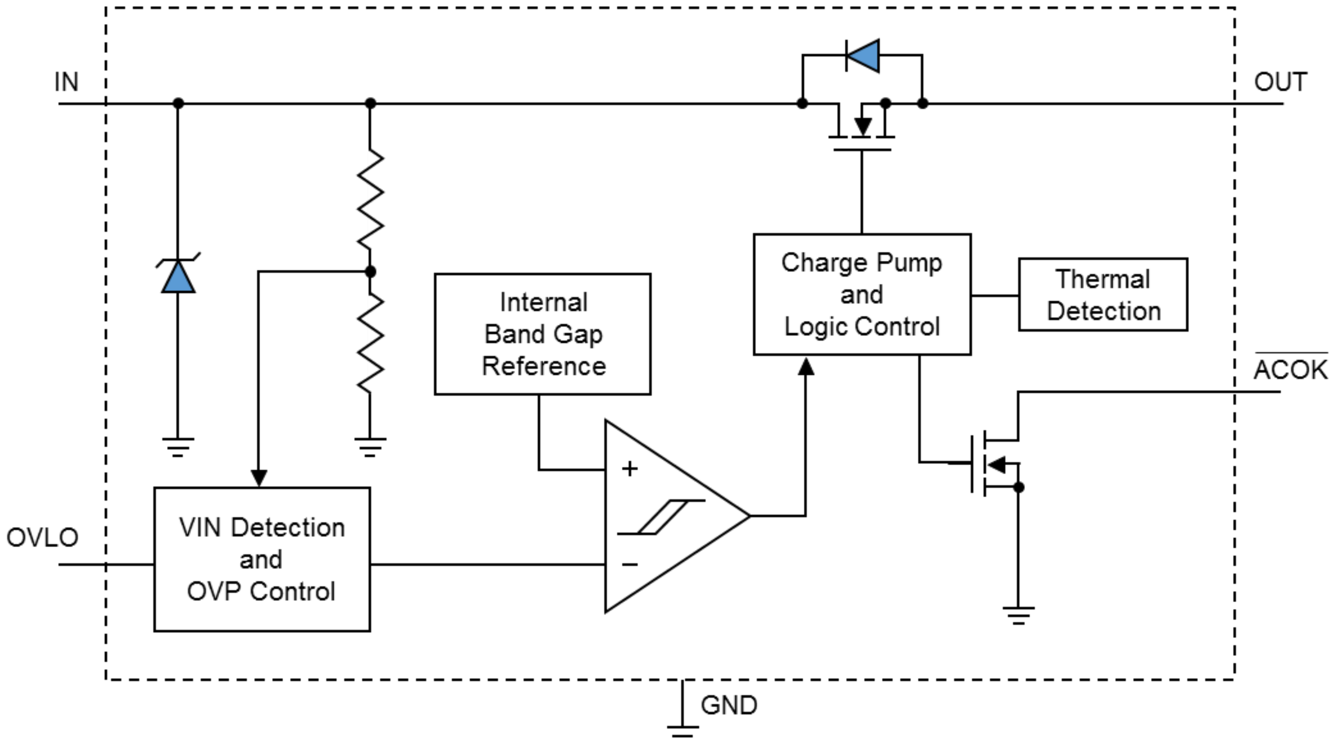
Over Voltage Fault Protection (VIN 5V to 8V step)



Surge Transient (110V)



Functional Block Diagram



Functional Description

The KTS1685 is inserted between the power supply or charger source and the load to be protected. The KTS1685 consists of a low resistance OVP switch, under-voltage lockout protection (UVLO), over-voltage monitor and protection (OVLO), and a fault output flag.

The KTS1685 overvoltage protection devices feature a low on-resistance (R_{DSON}) internal FET and protect low-voltage systems against voltage faults up to +30VDC. An internal clamp also protects the devices from surges up to +100V. If the input voltage exceeds the overvoltage threshold, the internal FET is turned off to prevent damage to the protected components. The 15ms debounce time built into the device prevents false turn on of the internal FET during startup.

In normal operation the OVP switch acts as a slew-rate controlled load switch, connecting and disconnecting the power supply from IN to OUT. A low resistance N channel MOSFET is used as to minimize the voltage drop between the voltage source and the load and to reduce the power dissipation.

When the voltage on the input exceeds the programmed over-voltage trip point, the device immediately turns off the internal OVP switch disconnecting the load from the abnormal voltage, preventing damage to any downstream components.

In the event that the power dissipation causes the chip temperature to exceed its maximum temperature setting, the KTS1685 will switch off protecting the device. Once the chip temperature has cooled to below the hysteresis temperature, KTS1685 will re-initiate. Should the over-temperature condition persist, then KTS1685 will continue to thermally cycle on and off, until such time as the system shuts it down.

The KTS1685 has a fault flag ($\overline{\text{ACOK}}$) pin to indicate the fault conditions of input power under-voltage, over-voltage, and over-temperature by pulling the flag signal high to alert the system. If an input over-voltage condition exists at the time of the device enable, then the OVP switch will remain OFF and $\overline{\text{ACOK}}$ is always high.

UVLO (Under Voltage Lockout)

The device has a built-in under voltage lock out (UVLO) circuit. During V_{IN} positive going slope, the output remains disconnected from input until V_{IN} voltage is above 1.8V plus hysteresis nominal. This circuit has a 100mV hysteresis to provide noise immunity to transient condition.

OVLO (Over Voltage Lockout)

The KTS1685 adjustable version has a 1.22V (typ) overvoltage trip threshold on the OVP pin. With a resistor divider on OVP pin from IN to GND, the over-voltage protection point of IN can be adjusted between 4V and 22V. Fixed OVP products are also available where the resistive divider is internally integrated and 6.8V (typ) OVLO threshold trip voltage.

Internal MOSFET Switch

The KTS1685 incorporates an internal FET with a 140mΩ (typ) RON. The FET is internally driven by a charge pump that generates a necessary gate voltage above IN.

$\overline{\text{ACOK}}$ Output

The $\overline{\text{ACOK}}$ output is an active-high open-drain fault (OV/ OT) reporting output. A pull-up resistor should be connected from $\overline{\text{ACOK}}$to the logic I/O voltage of the system. $\overline{\text{ACOK}}$ is normally high indicating the presence of an under-voltage, over-voltage, or over-temperature fault. Only when the switch is in normal operation will the $\overline{\text{ACOK}}$ pin be pulled to ground, indicating “power good”.

Thermal Protection

The internal FET turns off when the junction temperature exceeds +135°C (typ). The device exits thermal shutdown after the junction temperature cools by 20°C (typ).

Application Information

Input Capacitor

A 0.1μF or larger capacitor is typically recommended for CIN. CIN should be located as close to the device IN pin as practically possible. There is no specific capacitor equivalent series resistance (ESR) requirement for CIN. For higher current operation, ceramic capacitors are recommended for CIN due to their inherent capability over tantalum capacitors to withstand input current surges from low impedance sources such as batteries in portable devices. Capacitors are typically manufactured in different voltage ratings. If the maximum possible surge voltage is known, select capacitors with a voltage rating at least 5V higher than the maximum possible surge voltage. 50V rated capacitors are generally good for most OVP applications to prevent any surge voltage.

Output Capacitor

In order to insure stability while current limit is active, a small output capacitance of approximately 1μF is required at the output. Likewise, with the output capacitor, there is no specific capacitor ESR requirement. If desired, COUT may be increased to accommodate any load transient condition.

External OVLO Adjustment

If OVLO is connected to ground, the internal OVLO comparator uses the internally set OVLO value.

If an external resistor-divider is connected to OVLO and VOVLO exceeds the OVLO select voltage, V_{OVLO_SELECT}, the internal OVLO comparator reads the IN fraction fixed by the external resistor divider.

R1 = 1MΩ is a good starting value for minimum current consumption. Since V_{IN_OVLO}, V_{OVLO_THRESH}, and R1 are known, R2 can be calculated from the following formula:

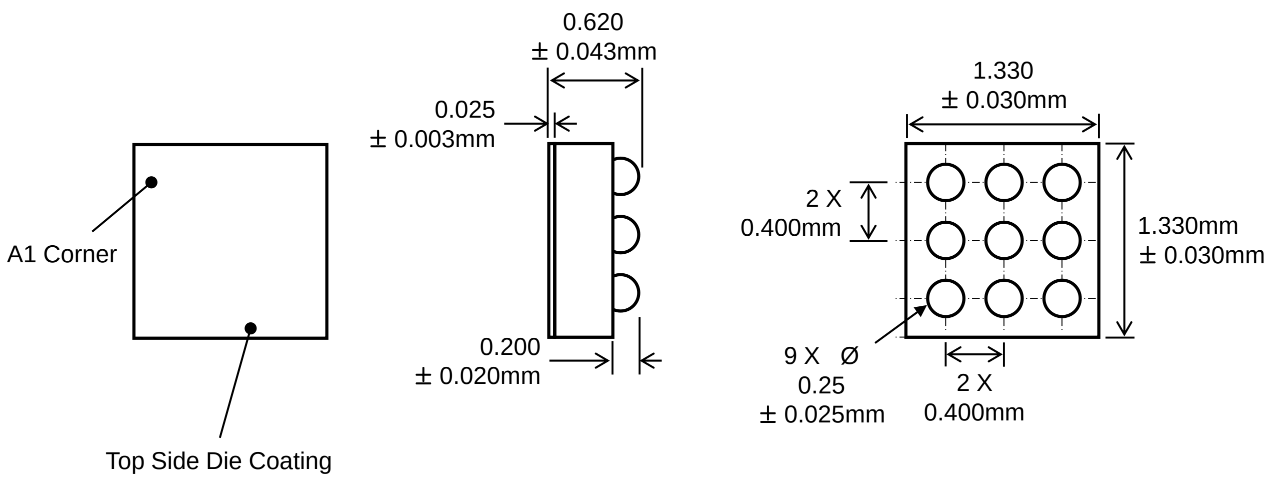
$$V_{IN\_OVLO} = V_{OVLO\_TH} \times (1 + \frac{R_1}{R_2})$$

This external resistor-divider is completely independent from the internal resistor-divider.

Packaging Information

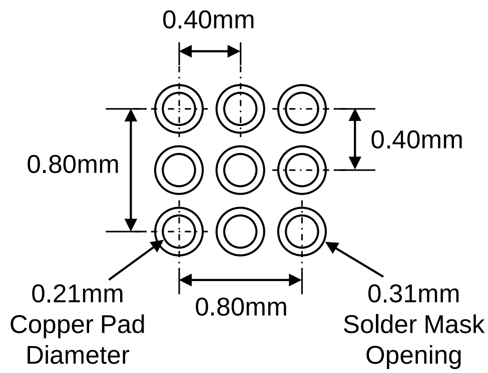
WLCSP - 9

Top View **Side View** **Bottom View**



Recommended Footprint

(NSMD Pad Type)



* Dimensions are in millimeters.