## How to use KTX9302 \& KTX9602 Motor Control with Power Integrations ${ }^{\text {TM }}$ BridgeSwitch ${ }^{\text {TM }}$

## Introduction

Both KTX9302 and KTX9602 are motor driver controller IC and support direct status communication with Power Integrations ${ }^{\top \mathrm{M}}$ BridgeSwitch ${ }^{\top \mathrm{M}}$ products. This application note is to describe the operation of relative registers in KTX9302 and KTX9602, and application diagrams are listed for reference.

## Functional Description

## Pin Assignment

The KTX9302 has one dedicated pin to connect with BridgeSwitch ${ }^{\text {TM }}$ FAULT pin, and KTX9602 has 2 dedicated pins for the connection with BridgeSwitch ${ }^{\text {TM }}$ FAULT pin.
Pin 29 of KTX9302 is defined as BS_FAULT1 when using with BridgeSwitch ${ }^{\text {TM }}$.
Pin 45 of KTX9602 is defined as BS_FAULT1 and Pin 44 is defined as BS_FAULT2 when using with BridgeSwitch ${ }^{\text {TM }}$.

## Register Map

| Hex <br> Address | Name | Type | Access | Default Reset | B7 | B6 | B5 | B4 | B3 | B2 | B1 | B0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| 0x00 | Status | Status | R | 10000000 | Run | bs_fault | OT | g_fault[1:0] |  | over_curr[2:0] |  |  |
| $0 \times 01$ | Config | Config | R/W | 00000000 | bs_start | bs_config | Fb_config | Motor_config[1:0] |  | BS_shut | BS_enable[1:0]- |  |
| 0xEC | Bs_status 11 | Status | R | 00000000 | Bs_status11[7:0] |  |  |  |  |  |  |  |
| 0xED | Bs_status12 | Status | R | 00000000 | Bs_status12[7:0] |  |  |  |  |  |  |  |
| 0xEE | Bs_status13 | Status | R | 00000000 | Bs_status13[7:0] |  |  |  |  |  |  |  |
| 0xEF | Bs_status21 | Status | R | 00000000 | Bs_status21[7:0] |  |  |  |  |  |  |  |
| 0xF0 | Bs_status22 | Status | R | 00000000 | Bs_status22[7:0] |  |  |  |  |  |  |  |
| 0xF1 | Bs_status23 | Status | R | 00000000 | Bs_status23[7:0] |  |  |  |  |  |  |  |

## Application information

## Config (0x01)

Config is the read-write register for BridgeSwitch ${ }^{\top}$ 解 function setting, except setting up the configuration of KTX9302 and KTX9602.

| Register | Address | Bit |  |  |  |  |  |  |  |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
|  |  | $\mathbf{7}$ | $\mathbf{6}$ | $\mathbf{5}$ | $\mathbf{4}$ | $\mathbf{3}$ | $\mathbf{2}$ | $\mathbf{1}$ | $\mathbf{0}$ |
| Config[7:0] | 01 h | bs_start | bs_config | Fb_config | motor_config[1:0] | BS_shutdown | BS_enable[1:0] |  |  |

## bs_start: Start status requesting of BridgeSwitch ${ }^{\text {TM }}$

Set "bs_start" bit to " 1 " is requesting all BridgeSwitch ${ }^{\text {TM }}$ parts to update the current status or reset then update status, according to bs_config bit setting.

The "bs_start" will automatic clear after sending out the request though "BS_FAULT1" and "BS_FAULT2" pins. technologiesw
bs_config: BridgeSwitch ${ }^{\text {TM }}$ status request configuration
Set "0" for reset all bridge switch and update the status.
Set " 1 " for update current status only.

BS_shutdown: BridgeSwitch ${ }^{\text {TM }}$ Fault Shutdown Enable
Enable the shutdown function for BridgeSwitch ${ }^{\text {TM }}$ protection
0 : Disable BS Shutdown
1 : Enable BS Shutdown
The fault action detail is shown on below table.

| BridgeSwitch ${ }^{\text {TM }}$ Fault | Fault ID | KTX9302/KTX9602 <br> Action |
| :---: | :---: | :---: |
| Device Ready | 0000000 | None |
| HV Bus Over Voltage | $001 \times x x x$ | Shutdown / Warning |
| HV 100\% | $010 x x x x$ | Warning |
| HV Bus 85\% | $011 x x x x$ | Warning |
| HV Bus 70\% | $100 x x x x$ | Warning |
| HV Bus 55\% | $101 \times x x x$ | Warning |
| System Thermal | $110 x x x x$ | Shutdown / Warning |
| LS Driver Not Ready | 111 xxxx | Shutdown / Warning |
| LS FET Thermal Warning | xxx010x | Warning |
| LS FET Thermal Shutdown | xxx10xx | Shutdown / Warning |
| LS FET Over-Current | xxxxx1x | Shutdown / Warning |
| HS Driver Not Ready | xxx11xx | Shutdown / Warning |
| HS FET Over-Current | xxxxxx1 | Shutdown / Warning |

BS_enable [1:0]: BS_FAULT1/2 pin enable

| BS_enable[ [1] | BS_enable[ [0] | Description |
| :---: | :---: | :--- |
| 0 | 0 | No BridgeSwitch ${ }^{\text {TM }}$ in use |
| 1 | 0 | BS_FAULT1 is used |
| 0 | 1 | BS_FAULT2 is used |
| 1 | 1 | Both of BS_FAULT1 and BS_FAULT2 are used |

## Description of BridgeSwitch ${ }^{\text {TM }}$ Status

1. The corresponding relations between the Power Integrations ${ }^{T M}$ BridgeSwitch ${ }^{T M}$ Device ID and BS_Stauts_xx is as below:

| ID 1/Ch1 | ID 2/Ch1 | ID 3/Ch1 | ID 1/Ch2 | ID 2/Ch2 | ID 3/Ch2 |
| :---: | :---: | :---: | :---: | :---: | :---: |
| BS_Status_11 | BS_Status_12 | BS_Status_13 | BS_Status_21 | BS_Status_22 | BS_Status_23 |

Below table lists the device ID of Power Integrations ${ }^{T M}$ BridgeSwitch ${ }^{T M}$ part, resulting device ID time period $t_{10}$, and how to program the respective ID through ID pin connection.

| Device ID | $\mathbf{t}_{\mathbf{I D}}$ | ID Pin <br> Connection |
| :---: | :---: | :---: |
| 1 | $40 \mu \mathrm{~s}$ | BPL Pin |
| 2 | $60 \mu \mathrm{~s}$ | Floating |
| 3 | $80 \mu \mathrm{~s}$ | SG Pin |

Device ID Selection through ID Pin.
2. The corresponding relations between BS_Status_xx and Power Integrations ${ }^{T M}$ BridgeSwitch ${ }^{\text {TM }}$ part's status is as below:

| BIT7 | BIT6 | BIT5 | BIT4 | BIT3 | BIT2 | BIT1 | BIT0 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| BrSw Exist | BrSw <br> Bit0 | BrSw | Bit1 | BrSw | Bit2 | BrSw | Bit3 | | Bit4 |
| :---: |

3. The details of BridgeSwitch ${ }^{T M}$ status are as below:

| BridgeSwitch ${ }^{\text {TM }}$ FAULT | Bit 0 | Bit 1 | Bit 2 | Bit 3 | Bit 4 | Bit 5 | Bit 6 |
| :---: | :---: | :---: | :---: | :---: | :---: | :---: | :---: |
| HV bus OV | 0 | 0 | 1 |  |  |  |  |
| HV bus UV 100\% | 0 | 1 | 0 |  |  |  |  |
| HV bus UV 85\% | 0 | 1 | 1 |  |  |  |  |
| HV bus UV 70\% | 1 | 0 | 0 |  |  |  |  |
| HV bus UV 55\% | 1 | 0 | 1 |  |  |  |  |
| System thermal fault | 1 | 1 | 0 |  |  |  |  |
| S Driver not ready ${ }^{1}$ | 1 | 1 | 1 |  |  |  |  |
| LS FET thermal warning |  |  |  | 0 | 0 |  |  |
| LS FET thermal shutdown |  |  |  | 1 | 0 |  |  |
| HS Driver not ready ${ }^{2}$ |  |  |  | 1 | 1 |  |  |
| LS FET over-current |  |  |  |  |  | 1 |  |
| HS FET over-current |  |  |  |  |  |  | 1 |
| Device Ready (no faults) | 0 | 0 | 0 | 0 | 0 | 0 | 0 |

1. Includes XL pin open/short-circuit fault, IPH pin to XL pin short circuit, and trim bit corruption.
2. Includes HS-to-LS communication loss, VBPH or internal 5 V rail out of range, and XH pin open/short-circuit fault. technologies ${ }_{\text {т }}$

## Typical Application Diagrams

## 3-wire Half-Bridge Application Circuit



Figure 1. KTX9302 3-wire Motor Driver with BridgeSwitch ${ }^{\text {TM }}$

## 6 -wire Full-Bridge Application Circuit ${ }^{3}$



Figure 2. KTX9602 6-wire Motor Driver with BridgeSwitch ${ }^{\text {TM }}$

## Related Documentation

1. Kinetic Technologies Datasheet: KTX9302, KTX9602 Datasheet
